Lecture 10:
Latch and Flip-Flop Design

Slides orginally from:
Vladimir Stojanovic

Computer Systems Laboratory
Stanford University
horowitz@stanford.edu

Outline

- Recent interest in latches and flip-flops
- Timing and Power metrics
- Design and optimization tradeoffs
- Master-slave vs. Pulse-triggered Latch
- Representative designs
- Comparison

Recent Interest in Flip-Flops

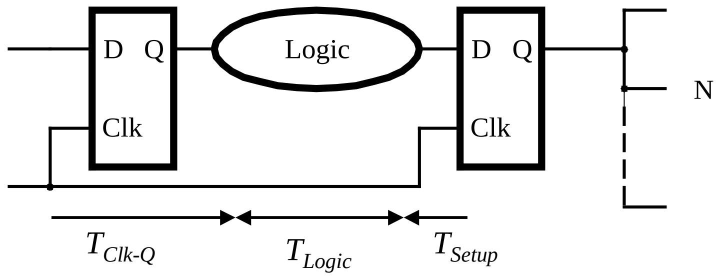
- Trends in high-performance systems
  - Higher clock frequency
  - More transistors on chip
- Consequences
  - Increased flip-flop overhead relative to cycle time
    - Cycle time 10 - 20 FO4 delays, flop overhead 2 - 4 FO4
  - Difficult to control both edges of the clock
  - Higher impact of clock skew
  - Higher crosstalk and substrate coupling
  - Higher power consumption
    - expensive packages and cooling systems
    - limit in performance
  - Clock burns up to 40%, flops up to 20% of total power

Requirements in the Flip-Flop Design

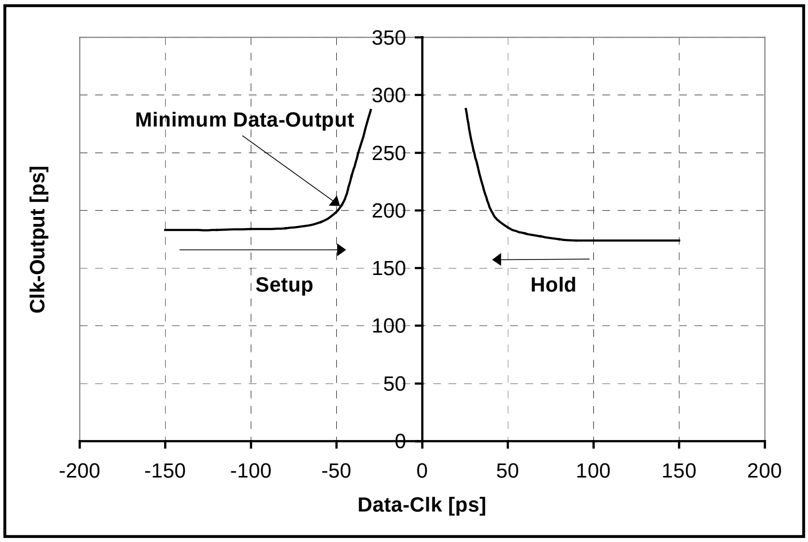
- Small Clk-Output delay, Narrow sampling window
- Low power
- Small clock load
- High driving capability (increased levels of parallelism)
  - Typical flip-flop load in a 0.18μm CMOS ranges from 50fF to over 200fF, with typical values of 100-150fF in critical paths (2-8FO4s or even higher)
- Integration of logic into the flop
- Multiplexed or clock scan
- Crosstalk insensitivity
  - dynamic/high impedance nodes are affected

Flip-Flop Delay

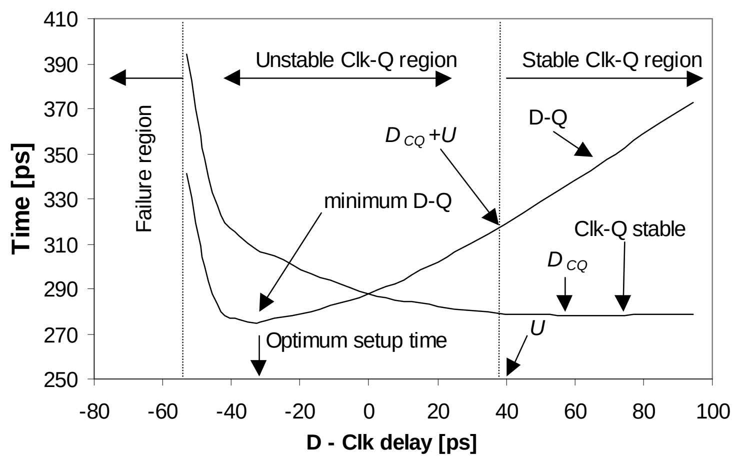
- Sum of setup time and Clk-output delay is the only true measure of the performance with respect to the system speed
- $T = T_{Clk\text{-}Q} + T_{Logic} + T_{setup} + \mathrm{T}_{skew}$



Delay vs. Setup/Hold Times

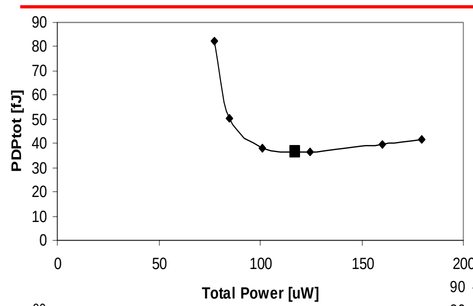


Timing parameters, details

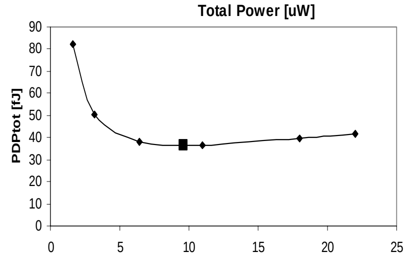


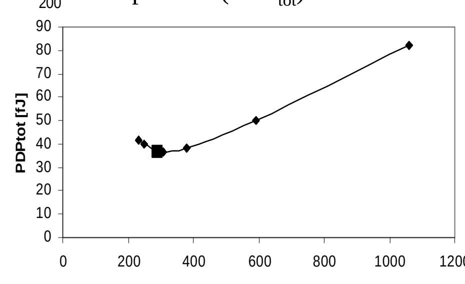
The best point to pick on delay curve is **minimum D-Q**

Design & optimization tradeoffs



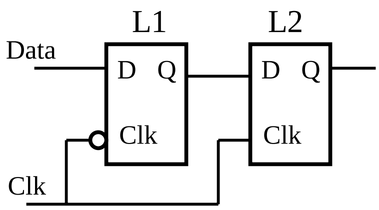
- Opposite Goals
  - Minimal Total power consumption
  - Minimal Delay
- Power-Delay tradeoff
- Minimize Power-Delay product (PDP_{tot})



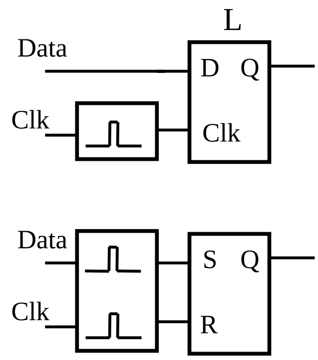


Types of Flip-Flops

Master-Slave Latch



Pulse-Triggered Latch

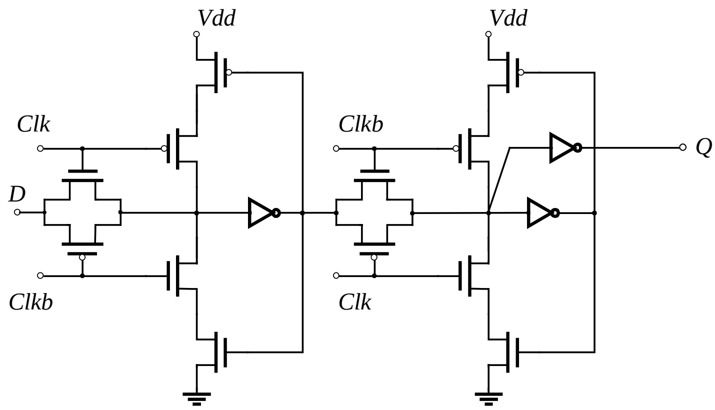


Master-Slave Latches

- Positive setup times
- Two clock phases:
  - distributed globally
  - generated locally
- Small penalty in delay for incorporating MUX
- Some circuit tricks needed to reduce the overall delay

T-G Master-Slave Latch

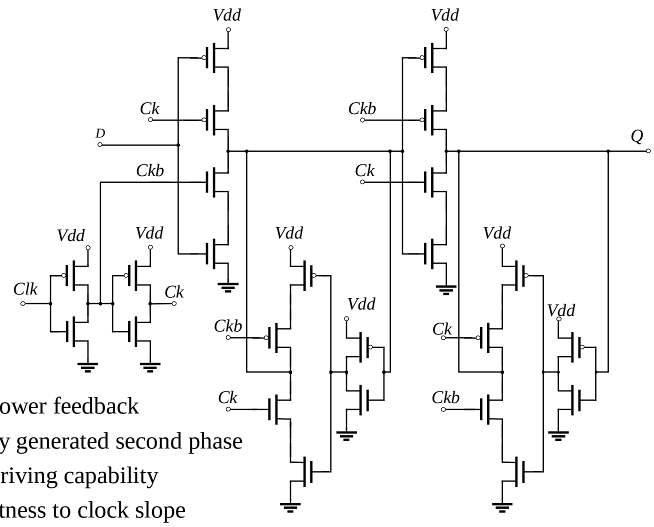
- PowerPC 603 (Gerosa, JSSC 12/94)



T-G Master-Slave Latch

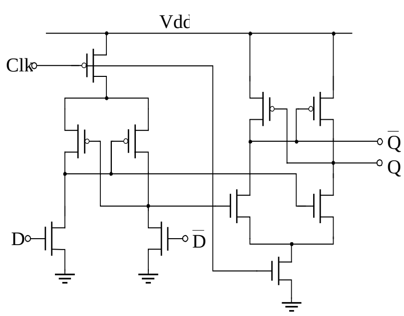
- Low power feedback
- Unbuffered input
  - input capacitance depends on the phase of the clock
  - over-shoot and under-shoot with long routes
  - wirelength must be restricted at the input
- Clock load is high
- Low power
- Small clk-output delay, but positive setup
- Easily embedded scan or mux

C^2MOS MS Latches

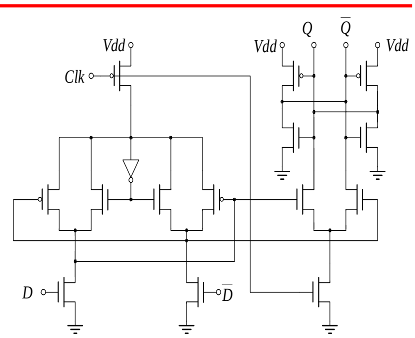


- Low power feedback
- Locally generated second phase
- Poor driving capability
- Robustness to clock slope

Single-Transistor-Clocked MS latches



DSTC



SSTC

- Yuan and Svennson, JSSC Jan. ‘97
- Ratioed DCVS and SRPL based designs
- Relatively small clock load
- Very sensitive to input glitching
- Capacitive coupling and charge sharing related speed and power problems

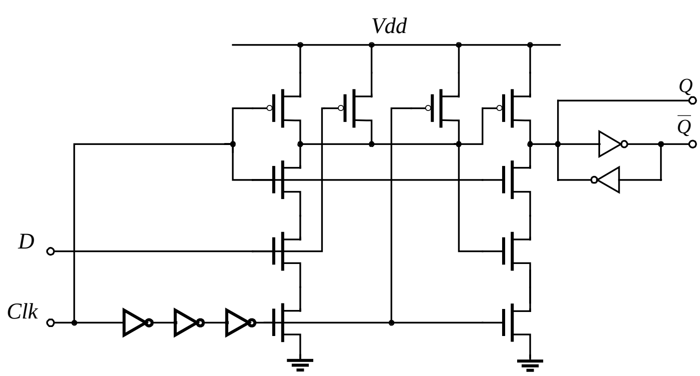
Pulse-Triggered Latches

- First stage is a pulse generator
  - generates a pulse (glitch) on a rising edge of the clock
- Second stage is a latch
  - captures the pulse generated in the first stage
- Pulse generation results in a negative setup time
- Frequently exhibit a soft edge property
- Must check for hold time violations

Note: power is always consumed in the clocked pulse generator

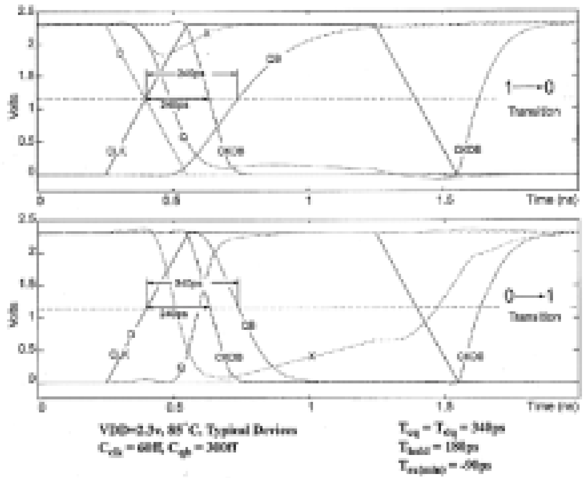
Hybrid Latch Flip-Flop

- AMD K-6, Partovi, ISSCC'96



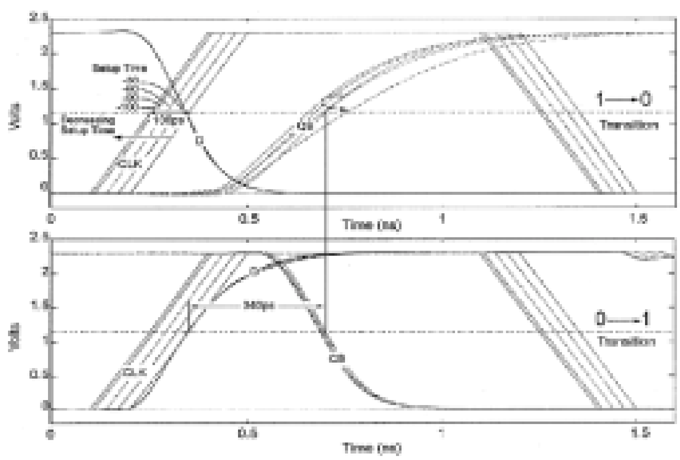
HLFF Operation

- 1-0 and 0-1 transitions at the input with 0ps setup time



Hybrid Latch Flip-Flop

Skew absorption



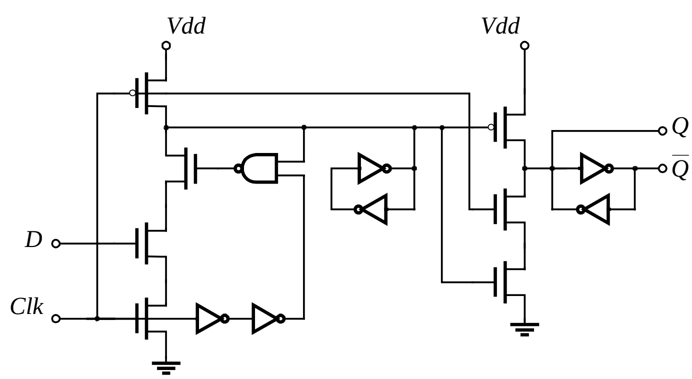
Partovi *et al*, ISSCC'96

Hybrid Latch Flip-Flop

- Flip-flop features:
  - single phase clock
  - edge triggered, on one clock edge
- Latch features: Soft clock edge property
  - brief transparency, equal to 3 inverter delays
  - negative setup time
  - allows slack passing
  - absorbs skew
- Hold time is comparable to HLFF delay
  - minimum delay between flip-flops must be controlled
- Fully static
- Possible to incorporate logic

Semi-Dynamic Flip-Flop (SDFF)

- Sun UltraSparc III, Klass, VLSI Circuits'98

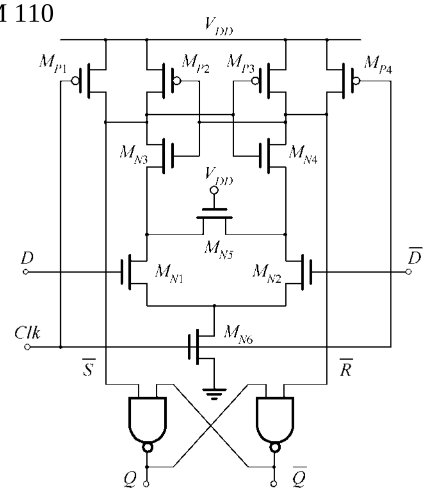


- Soft edge conditioned by data since first stage is precharged - cross-coupled latch is added for robustness
- Small penalty for adding logic
- Latch has one transistor less in stack - faster than HLFF, but 1-1 glitch exists

Sense-amplifier-based flip-flop

Matsui et al. 1994.
DEC Alpha 21264, StrongARM 110

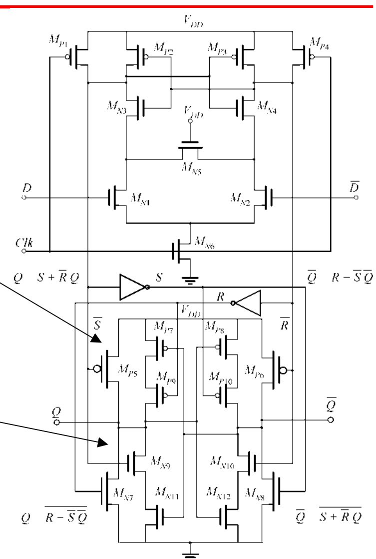
- First stage is a sense amplifier
- On rising clock edge monotonic S_b or R_b trigger the S-R latch
- Cross-coupled NAND - speed bottleneck
- Big power savings in reduced swing designs
- Nice interface to/from domino logic



Modified Sense Amplifier-Based Flip-Flop

- The first stage is unchanged sense amplifier
- Second stage is sized to provide maximum switching speed
- Driver transistors are large
- Keeper transistors are small and disengaged during transitions

Nikolic & Stojanovic, ISSCC '99



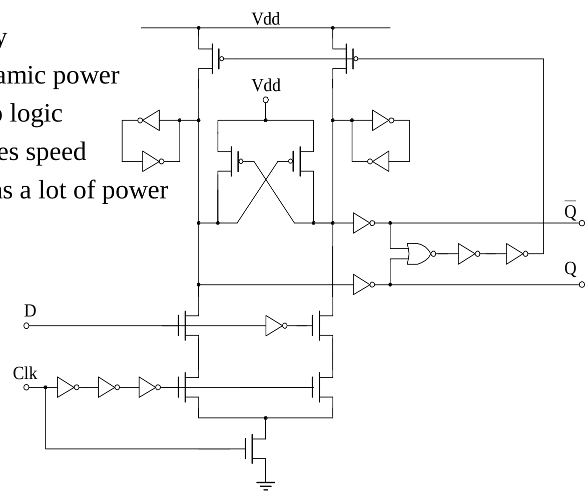
Modified Sense Amplifier-Based Flip-Flop

- Delay of each of the outputs is independent of the load on the other output
- Delay of Q and $\overline{Q}$ is symmetrical as opposed to the NAND based design
- Convenient for dual rail logic and driving strength for standard CMOS is effectively doubled
- SAFF presents a small clock load, small setup time and all the advantages of original design

- Possible tradeoff between speed and robustness to cross-talk

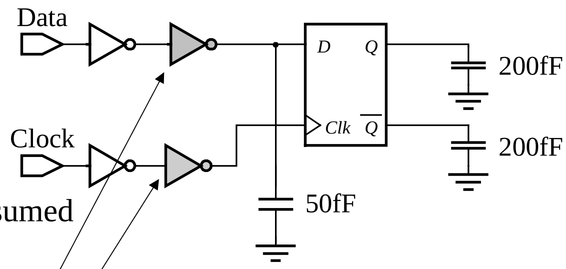
K-6 Dual-Rail ETL

- Self-reset property
  - increases dynamic power
  - drives domino logic
- Precharge increases speed
- Very fast but burns a lot of power
- Small clock load



Flip-Flop Performance Comparison

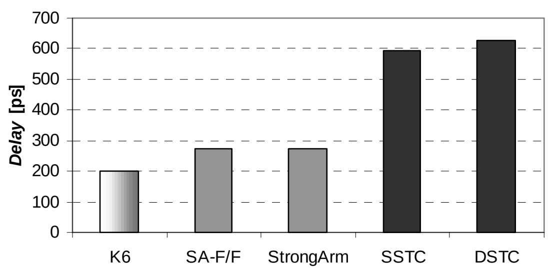
Test bench

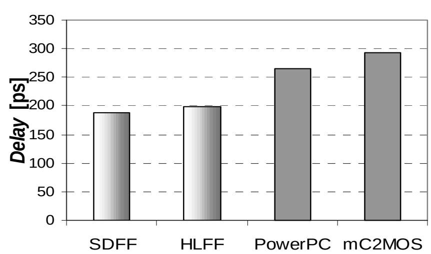


- Total power consumed
  - internal power
  - data power
  - clock power
- Measured for four cases
  - no activity (0000… and 1111…)
  - maximum activity (0101010..)
  - average activity (random sequence)

Delay is (minimum *D-Q*)
Clk-Q + setup time

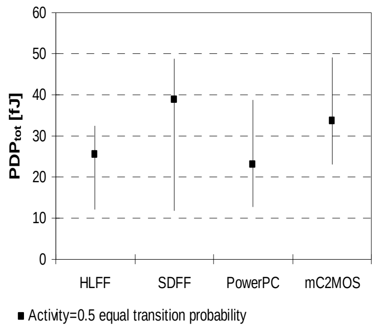
Delay comparison

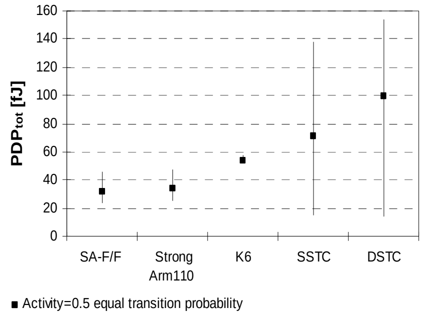




- Pulsed design brings the fastest structures

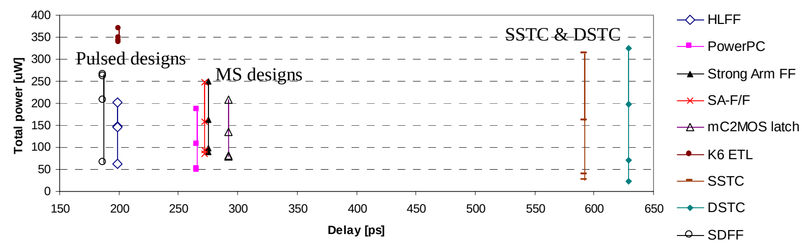
Overall performance

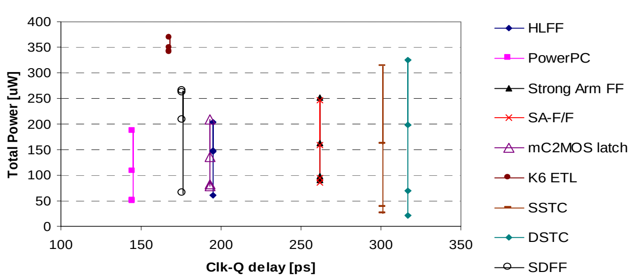




- Real signals have the activity between 0 and 0.5 (■)
- Precharged hybrid structures are the fastest but their power consumption strongly depends on the probability of "ones"
- More "ones" above the ■ point

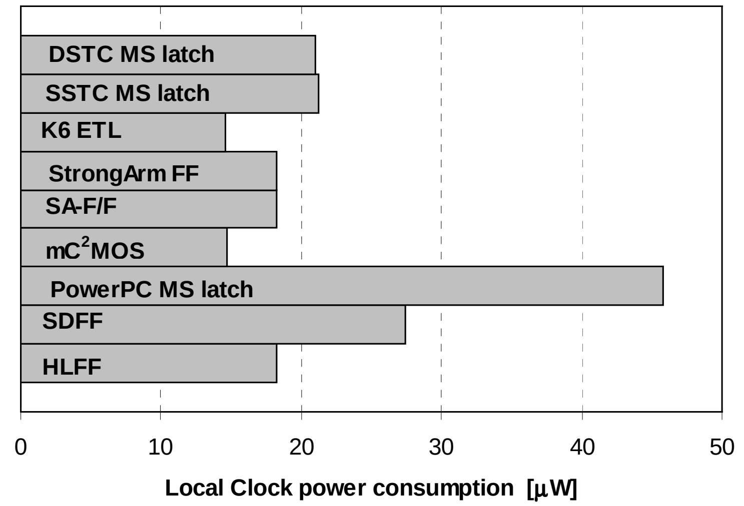
Conventional Clk-Q vs. minimum D-Q





- Hidden positive setup time
- Degradation of total delay

Comparison of Clock power consumption



Design goals

- Apply
  - Small clock load
  - Short direct path
  - Reduced node swing
  - Low-power feedback
  - Pulsed design
  - Optimization of both Master and Slave latch
- Avoid
  - Positive setup time
  - Sensitivity to clock slope and skew
  - Dynamic (floating) nodes
  - Dynamic Master latch

Conduct Power *Delay optimizations on constant frequency - really optimize Energy*Delay product

Take into account all sources of power dissipation

ALWAYS use Clk-Q + setup time for max delay

General characteristics

- 60ps = FO4 delay in .2u technology
- min gate width 1.6u

Table 1: General characteristics

Nominal conditions	# of transistors	Total transistor width [u]	Internal power [uW]	Clock power [uW]	Data power [uW]	Total power [uW]	Delay [ps]	PDP_{tot} [fJ]
PowerPC 603	16	147	36	46	5	87	266	23
HLFF	20	162	106	18	3	127	199	25
SDFF	23	167	158	27	2	187	187	35
mC^2MOS	24	170	94	15	6	115	292	34
SA-F/F	19	214	97	18	3	118	272	32
StrongArm FF	20	215	101	18	3	122	275	34
K6 ETL	37	246	250	15	5	270	200	54
SSTC	16	147	94	22	4	120	592	71
DSTC	10	136	132	22	4	158	629	99