

## TUTORIAL 1

# SystemC: From Language to Applications, From Tools to Methodologies

### Speaker:

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### Abstract

This tutorial will cover SystemC from more than just a language perspective. It will start with a brief survey of language features and capabilities, including some of the more recent developments such as the SystemC Verification Library. The usage of several of these language features, in particular for system-level modeling, design, verification and refinement will be illustrated. We will then address many interesting applications of SystemC drawn from a number of different industrial and academic research groups.

Next, we will talk about current tools available for design modeling, analysis and implementation with SystemC, covering the areas of co-simulation, synthesis, analysis, refinement, and testbenches, illustrating them with examples. Of course, tools are not enough; we will cover a number of methodology examples, in particular illustrating the use of SystemC in building complete design flows for complex SoC and system designs. This will also illustrate the linkage between SystemC and other design languages. We will close with a few notes on possible future SystemC evolutions.