

SystemC based Hardware Synthesis Becomes Reality

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Abstract

The advances in ASIC technology have enabled the design of systems-on-chip (SoC). The complexity associated with SoC is creating many new challenges at all levels of the design process. At the systems level, engineers are reconsidering how designs are specified, partitioned and verified. Systems and software engineers have adopted tools and methodologies based on C/C++ programming language, whereas their hardware counterparts are almost exclusively using hardware description languages such as VHDL and Verilog. This is one obvious reason for the communication gap that exists between different members of the same teams.

To overcome this basic problem, SystemC, an open community C++ modeling platform for system-level design and hardware/software co-design has been created. SystemC is broadly supported by a large and growing number of leading system houses, semiconductor companies, intellectual property (IP) providers, embedded systems and EDA tool vendors through the Open SystemC Initiative (OSCI). The objective of the OSCI is to engender a whole new market for system-level design solutions, based on its support of SystemC and a common modeling platform with built-in interoperability.

In order to gain acceptance from the SoC engineering community, the new standard modeling platform has to be more than just a means of communication; it has to support all kinds of features that can help to solve their most burning issue, namely "time-to-market." For SoC, it is essential to support the re-use of intellectual property (IP), like hardware units, software, architectures, etc. for multiple designs. That in turn means the support of IP creation as well as IP integration.

In particular, hardware synthesis is a critical step for the creation of IP. Until recently, the synthesis tools required VHDL/Verilog descriptions as the design entry language, which of course was one good reason for hardware engineers not to adopt SystemC in their design flow.

In June 2000, Synopsys has introduced SystemC Compiler, a synthesis tool that allows to synthesize hardware IP from a synthesizable subset of SystemC, thereby removing one of the biggest hurdles for the adoption of SystemC by the hardware design community.

In my presentation, I will highlight some of the features of hardware synthesis from SystemC and put this in the context of a complete SystemC based SoC design flow.