Power Management Issues for Future Generation Microprocessors*

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Abstract: **By reducing the power supply voltage, faster, lower power consumption, and high integration density data processing systems can be achieved. The current generation high-speed CMOS processors (e.g. Alpha, Pentium, Power PC) are operating at above 300 MHz with 2.5 to 3.3 V output range. Future processors will be designed in the 1.1-1.8 V range, to further enhance their speed-power performance. These new generations microprocessors will present very dynamic loads with high current slew rates during transient. As a result, they will require a special power supply, Voltage Regulator Module (VRM), to provide well-regulated voltage. The VRMs should have high power densities, high efficiencies, and good transient performance. This paper addresses the critical technical issues to achieve this target for future generation microprocessors.**

I. INTRODUCTION

Evolutions in microprocessor technology pose new challenges for supplying power to these devices. The evolution began when the high-performance Pentium processor was driven by a non-standard, less-than 5 V power supply, instead of drawing its power from the 5-V plane on the motherboard [1].

In order to meet faster and more efficient data processing demands, modern microprocessors are being designed with lower voltage implementations. The processor supply voltage in future generation processors will decrease to 1.1 V ~ 1.8V. More devices will be packed on a single processor chip and the processors will operate at higher frequencies, beyond 1GHz. Therefore, microprocessors need aggressive power management. Future generation processors will draw current up to 50 A ~ 100 A [2]. These demands in turn require special power supplies, Voltage Regulator Modules (VRMs), to provide lower voltages with higher current capability for microprocessors.

As the speed of the processors increase, they significantly increase the dynamic loading of the VRM. Future microprocessors are expected to exhibit higher current slew rate of 5A/ns. These slew rates represent a severe problem for large load changes that are encountered when the systems transfer from the sleep mode to the active mode and vice versa. In this case, the parasitic impedance of the power supply connection to the load and the ESR and ESL of capacitors have a dramatic effect on VRM voltage [2]. If this impedance is not low enough, the supply voltage may fall out of the required range during the transient period. Moreover, the total voltage tolerance will be much tighter. Currently, the voltage tolerance is 5% (for 3.3 V VRM output, the voltage deviation can be ± 165mV). In the future, the total voltage tolerance will be 2% (for 1.1 V VRM output, the voltage deviation can only be ± 33 mV). All these requirements pose serious design challenges. Table 1 shows the specifications for present and future VRMs.

Table 1. Specifications for present and future VRM

	Present	Future
Output Voltage:	2.1~3.5V	1~3V
Load Current:	0.3~13A	1~50A
Output Voltage Tolerance:	± 5%	± 2%
Current Slew at decoupling Capacitors	1A/nS *	5A/ns

*: Current slew rate at today's VRM output is 30A/uS

Most of today's VRMs use conventional buck or synchronous rectifier buck topology. In future microprocessor applications, the limitations of these topologies are very clear. In order to maintain future voltage regulation requirements during the transient, more output filter and decoupling capacitors will be needed [3]. However, the space of the VRM and motherboard is very limited. Increasing capacitors is an impractical approach. In order to meet future specifications, VRM with significantly higher efficiency, higher power density and faster transient must be developed. On the other hand, an advanced integration approach is required to minimize the effect of connection and component parasitics.

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To achieve this target, a number of critical issues have to be addressed. For example, advanced power device and control technologies are needed for high efficiency and high frequency operation. Today's vertical power device technology can not provide acceptable conversion efficiency at multi-megahertz due to its high conduction and switching and gate drive losses. Innovative power system architectures also should be developed to meet the new performance envelope while offering a cost-effective solution. In this paper, advanced VRM topologies for fast transient response and low ripple voltage together with advanced packaging technologies for improving power density and thermal management are among these important issues to be addressed. In addition, the limitations of today's technologies, VRM topologies and power device, are analyzed.

II. Limitations of Today's Technologies

A. *Limitation of Present VRM Topologies*

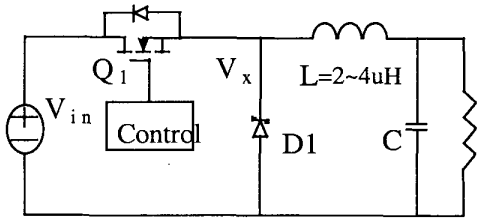


Fig. 1 Conventional Buck Converter

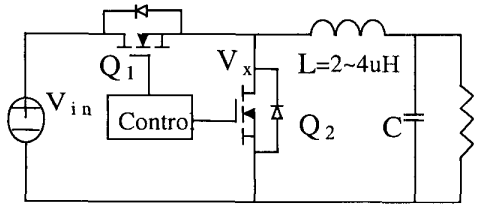


Fig.2 Synchronous Rectifier Buck

Most of today's VRMs use conventional buck or synchronous rectifier buck topology. Figure 1 shows the conventional buck circuit, which is the most cost-effective approach. Usually, Schottky diodes are used as a rectifier. The top MOSFET transfers energy from the input and the bottom rectifier conducts the inductor current. The control regulates the output voltage by modulating the conduction interval of the top MOSFET. Figure 2 shows the synchronous rectifier buck circuit. This topology increases the efficiency by replacing the rectifier with a low $R_{ds(on)}$ MOSFET. The synchronous switch is controlled by the complementary signal of the top switch's gate signal. The synchronous rectifier buck always operates in continuous current mode. Its transient response is faster than that of a conventional buck. Conventional VRMs use large output filter inductance, 2~4μH, to reduce ripple.

Figure 3 shows the practical VRM load model (processor model). The packaging capacitor is the parasitic capacitor inside the microprocessor package. There are a lot of decoupling capacitors near and around the microprocessors to reduce noise and maintain voltage regulation. Bulk capacitors are VRM output capacitors. All these capacitors have parasitic ESR and ESL. There are interconnection parasitic inductances and resistances between Bulk capacitors and decoupling capacitors and between decoupling capacitors and packaging capacitors. Future microprocessor load transitions will have 5A/ns-slew rate. In this case, all these parasitics have significant effect on VRM transient voltage. Figure 4 shows the transient response of a synchronous rectifier VRM. During the transient, there are three spikes in the voltage drop [3]. The first high frequency spike is dominated by loop 1, which combines the parasiric of the packaging capacitors and decoupling capacitors and the interconnection between them. The second spike is controlled by loop 2, which combines the parasitic of the decoupling capacitors and VRM bulk capacitors and the interconnection between them. The third spike is decided by loop 3, which is combines the parasitic of the VRM output filter inductor and bulk capacitors. In Figure 4, it can be determined that for future microprocessor load, today's VRM topologies can not meet the 2% transient requirement.

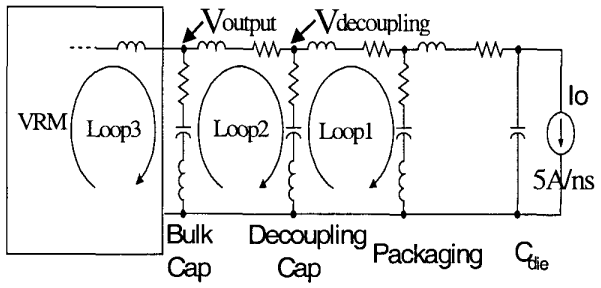


Fig. 3 Practical VRM load model

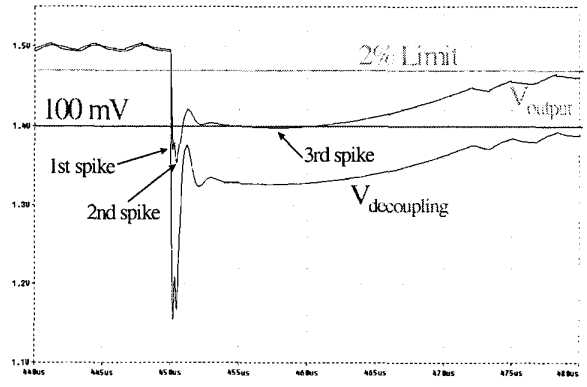


Fig.4 Transient response of conventional VRMs

The transient limitation of today's VRM topologies comes from their large output filter inductance. During the transient, this large inductor limits the energy transfer speed and the capacitors have to store or discharge all the energy from load. For future microprocessors, with heavier load currents, higher load transient slew rate and tighter voltage tolerance requirements, more decoupling capacitors are required to reduce the second spike, and more VRM output bulk capacitors are required to reduce the third spike. As a result, in order to meet future specifications, 23 times the decoupling capacitors are needed and 3 times VRM bulk capacitors are needed [3]. The VRM will be very big and expensive one. However, the space of VRM is very limited and the real estate of motherboard is very expensive. The need of a large quantity of capacitors makes the VRMs, which use these topologies, impractical for future microprocessors.

B. Limitation from power devices

Another limitation of the conventional VRM is efficiency. Figure 5 shows the conventional VRM efficiency at 2-V output. Using IRL3803 as switches, with an on-resistance of 6mΩ and 30 V voltage rating, the conventional VRM can not meet 80% efficiency requirement at heavy load. For lower output voltage, it will be even more difficult to meet the efficiency requirement. Figure 6 shows the conventional VRMs' efficiency at 1.2-V output. Their efficiency can not meet the 80% requirement for the whole load range.

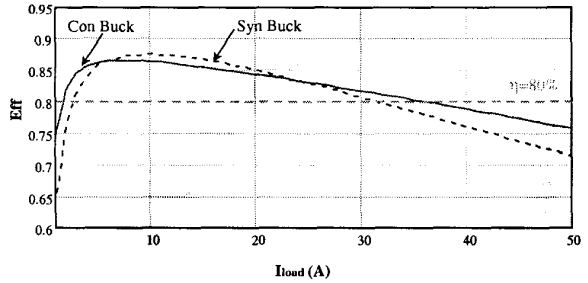


Fig. 5 Conventional VRM efficiency
(Vin=5V, Vo=2V, fs=300kHz, Switches: IRL3803)

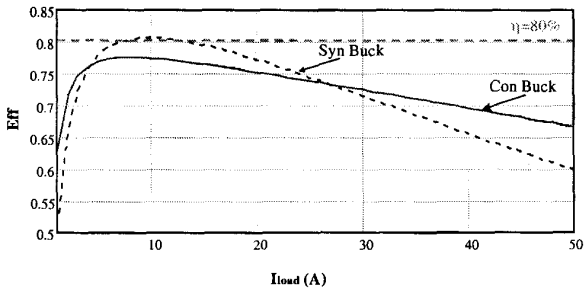


Fig. 5 Conventional VRM efficiency
(Vin=5V, Vo=1.2V, fs=300kHz, Switches: IRL3803)

This limitation is from today's power device's technology. Based on vertical power MOSFET technology, most of today's low-voltage power MOSFETs are available at a rating of 30 V. Roughly, the total power loss of a power device can be divided into three parts: 1) conduction loss; 2) gate drive loss and 3) switching loss. Figure 7 shows the relationship between conduction loss and gate drive plus switching loss. For this kind of low-voltage high-current application, conduction loss contributes a large percentage of the total loss. When only one IRL3803 is used, the MOSFET's conduction loss is 25 times gate drive plus switching loss. To reduce conduction and total loss, more switches need to be paralleled. However, this does not necessarily mean that more parallel switches equals lower total loss. When five IRL3803 are paralleled, the total loss is reduced to the minimum. After this point, adding more switches will not improve efficiency. Figure 8 shows the VRM efficiency with five IRL3803 in parallel. With the optimized efficiency design, the VRM's efficiency still can not meet the 80% requirement for the whole load range. This limitation is due to high Figure of Merit (FOM) of today devices. FOM is equal to Rdson times Qg. For today's device technology, the lowest FOM value is around 400 (mΩ × nC). With such a high FOM value, power devices not only limit the VRM's efficiency, but also limit the VRM's ability to operate at higher operating frequencies. Most of toady's VRMs operate at a switching frequency lower than 300 kHz. This low switching frequency causes slow transient response and very large energy storage components.

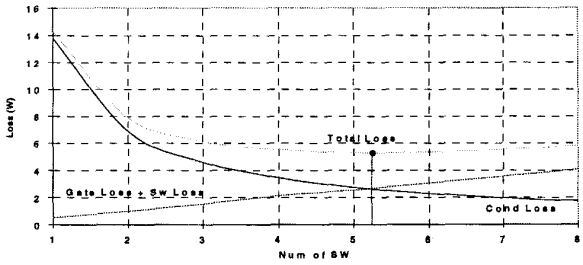


Fig. 7 Switching loss and gate drive loss and conduction loss of IRL3803 vs parallel switch number
(Vin=5V, fs=300kHz, Iload=50A)

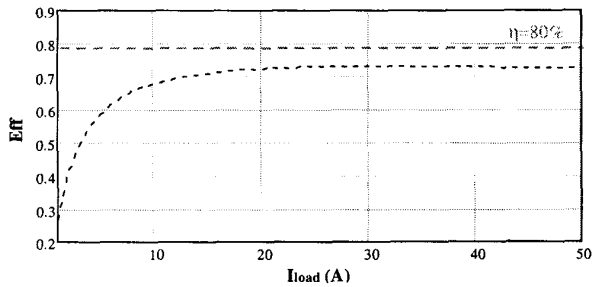


Fig. 8 Efficiency of synchronous buck VRM
(Vin=5V, Vo=1.2V, fs=300kHz, 5 IRL3803 in parallel)

III. ADVANCED VRM TOPOLOGIES

A. *Fast VRM topology*

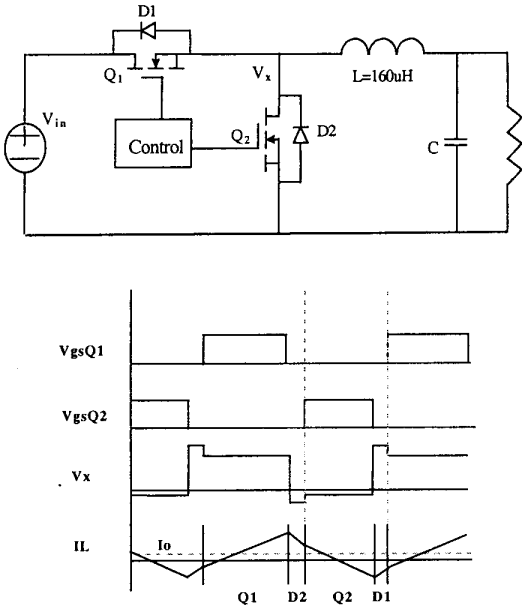


Fig. 9 Quasi-Square-Wave VRM topology

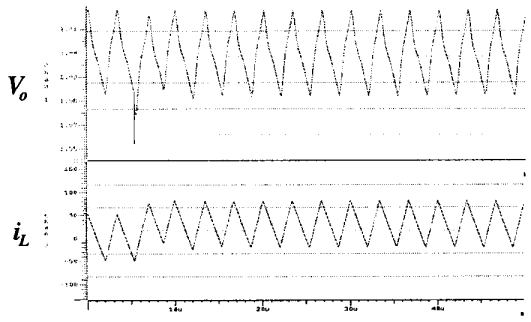


Fig. 10 Transient response of QSW

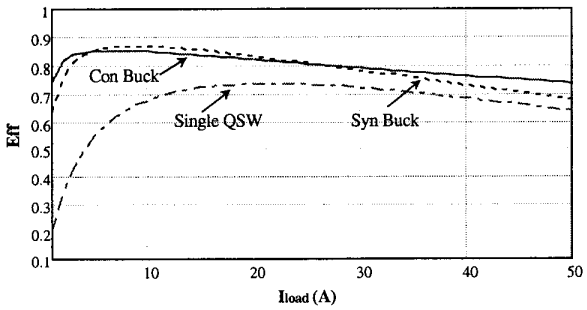


Fig. 11 Efficiency of QSW compared with conventional VRM
(Vin=5V, Vo=2V, fs=300kHz)

To overcome the transient limitation occurring in conventional VRMs, smaller output filter inductance is more desirable to increase the energy transfer speed. Figure 9 shows the Quasi-Square-Wave (QSW) circuit. The QSW topology keeps the VRM output inductor current touching zero in both 'sleep' and 'active' mode. When Q1 turns on, the inductor current is charged up by the input voltage to positive. After Q1 turns off and before Q2 turns on, the inductor current flows through Q2's body diode. When Q2 turns on, the inductor current is discharged to negative. After Q2 turns off and before Q1 turns on, the inductor current flows through Q1 body diode. Compared with conventional buck and synchronous buck topologies, its output filter inductance is reduced significantly. At 13 A load and 300 kHz switching frequency, it needs only a 160 nH inductor as compared with a 2~4 μH inductor used in the conventional design. This small inductance makes the VRM transient response much faster. Figure 10 shows the transient response of the QSW topology. The third spike in output voltage becomes insignificant and the second spike is reduced significantly.

There are two disadvantages of this fast VRM topology. The first one is the large current ripple. Huge VRM output filter capacitance is needed to suppress the steady state ripple. Smaller inductance results in faster transient response, but requires larger bulk capacitance. The second one is its low efficiency. In Figure 11, due to the large ripple current, QSW switches have larger conduction loss. Its efficiency is lower than that of conventional VRMs.

B. *Fast VRM with small ripple ---- interleaved QSW VRM*

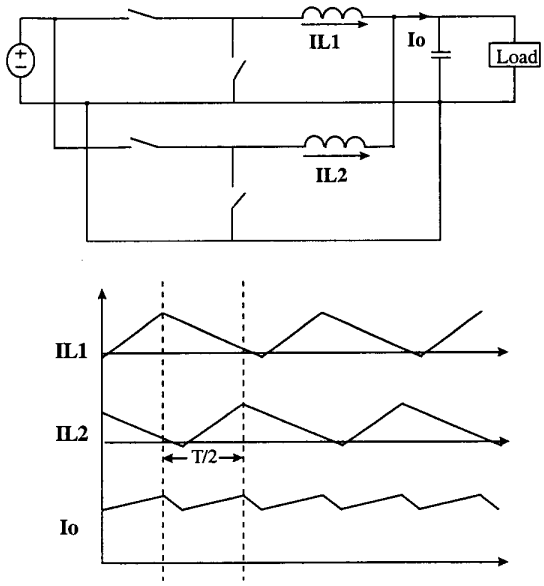


Fig. 12 Current ripple canceling effect of interleaved QSW

In order to meet both the steady state and transient requirements, a novel VRM topology, interleaved QSW, is introduced in Figure 12. The interleaved QSW topology naturally cancels the output current ripple and still maintains the fast transient response characteristics of the QSW topology. Smaller capacitance is needed as compared to both single-module QSW VRM and convention VRM design. The more the modules in parallel, the better the ripple canceling effect. Figure 13 shows a 4-module interleaved QSW VRM. Figure 14 shows its transient response. The result shows that this technique can meet future transient requirements without a large steady state voltage ripple. Compared with the single-module QSW topology, the efficiency is improved significantly. Figure 15 shows the efficiency comparison results.

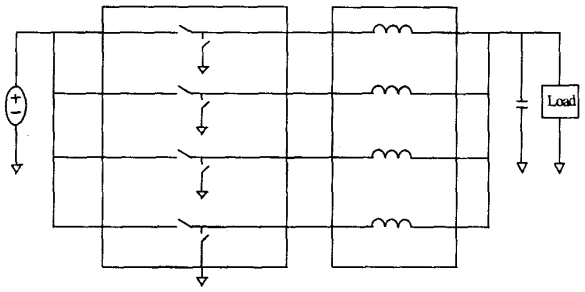
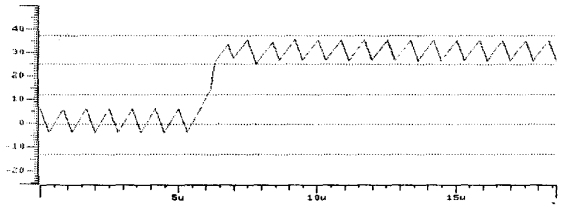
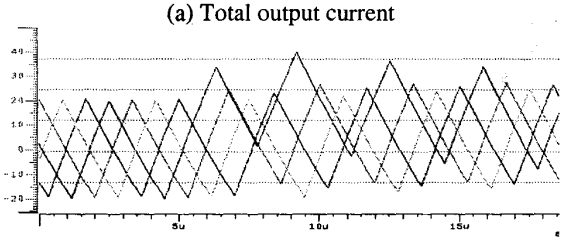


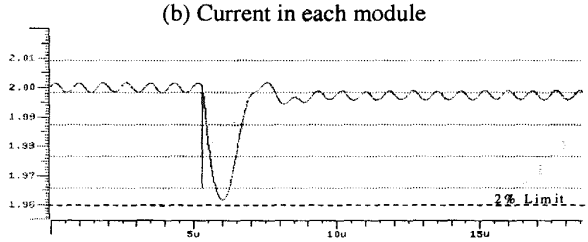
Fig. 13 4-module interleaved QSW VRM



(a) Total output current



(b) Current in each module



(c) Output voltage

Fig. 14 Transient response of 4-module interleaved QSW

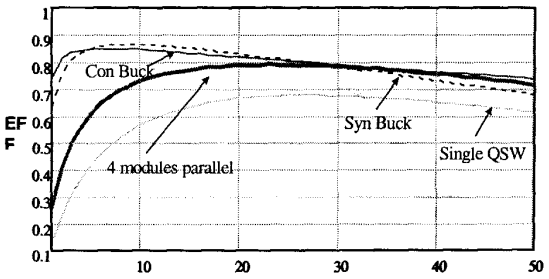
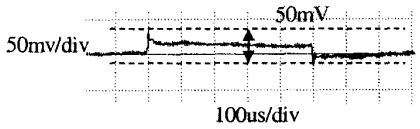


Fig. 15 Efficiency comparison

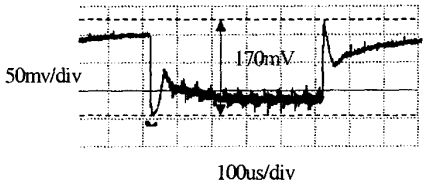
Interleaved QSW topology can not only reduce output current ripple, but can also reduce input current ripple. Table 2 compares the 4-module interleaved QSW VRM design with conventional VRM. Since the necessary capacitance is reduced, the VRM power density is dramatically increased. Also, since each module handles lower current, it will be packaged easier. Test results in Figure 16 show the transient response of 4-module interleaved QSW VRM and today's commercial VRM.

Table 2 Design comparison of Interleaved QSW VRM and Conventional VRM

	Interleaved QSW	Conventional VRM
Vin	5	5
Bulk capacitance	1200uF	8000uF
Output Inductance	320nH (×4)	3.8uH
Transient voltage drop:	50 mV	150 mV
Vo @ load	2V@30A	2V@13A
Power stage power Density (W/in^3)	30	3~5



(a) Transient response of 4-module interleaved QSW



(b) Transient response of conventional VRM

Figure 16. Transient response test results

IV. TECHNICAL BARRIER

------High efficient fast power device is required

In order to develop low-cost, high efficiency, low profile, high-power density, fast transient response, board-mount VRM modules for future generation microprocessor loads, high operating frequency is much more desirable. Figure 17 shows the transient response of interleaved QSW VRM when it operates at 1 MHz. Obviously, the voltage spike is reduced significantly. VRM density is also improved. Figure 18 shows the inductance and capacitance needed in interleaved QSW VRM when it operates at high switching frequency. At 10 MHz, the inductance needed is only 9.25 nH and the capacitance needed is only 5.26 μF.

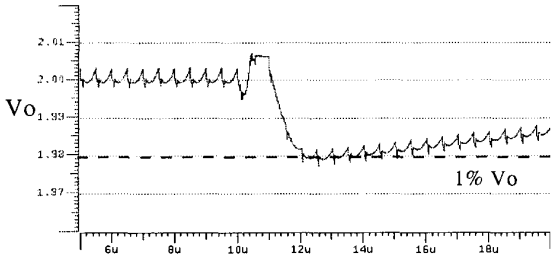
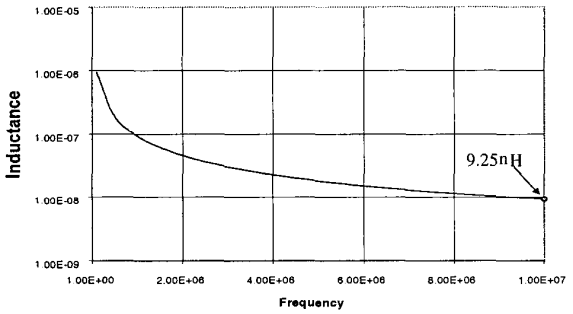
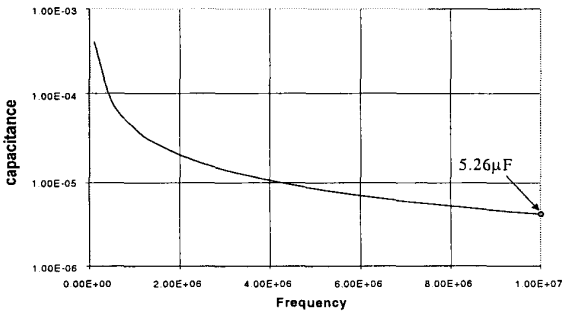


Fig. 17 Transient response of interleaved QSW
(Vin=5V, Vo=2v, fs=1MHz)



(a) Inductance needed vs. frequency



(b) Capacitance needed vs. frequency

Fig. 18 Inductance and capacitance needed in interleaved QSW VRM topology at high operating frequency

With such small inductance and capacitance, very high power density VRMs can be achieved and energy storage costs can be reduced dramatically. However, due to today's device technology, most VRMs operating frequency are lower than 300 kHz. Even at this frequency, the VRM can not meet the efficiency requirement (shown in Figure 15). If frequency is increased, VRM efficiency is shown in Figure 19. At 10 MHz, VRM will only have 40% efficiency. This efficiency makes thermal management and packaging very difficult.

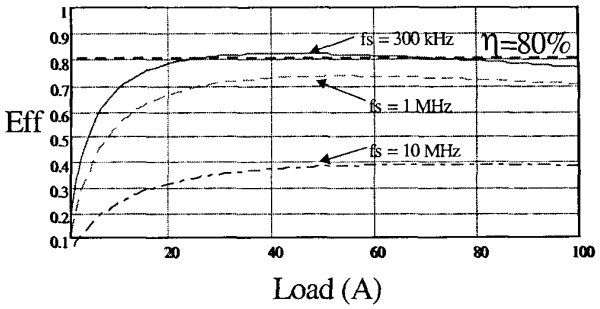


Fig. 19 VRM efficiency based on today's device
(Vin=5V, Vo=2V, Switches: 5 IRL3803 in parallel)

For future microprocessor application, the power device must have smaller FOM value (<100(mΩ × nC)) and lower miller charge. With improved device technology, for example SOI LDDMOS technology [4], future VRM efficiency will be higher than 90% at several MHz operating frequency. Its power density will be higher than 100 W/in^3. Table 3 shows the VRM efficiency comparison based on toady's device technology and improved LDDMOS technology.

Table 3 VRM Efficiency Comparison

Vin=5V, Vo=2V	BV (V)	FOM (mΩ*nC)	Optimized Efficiency For Interleaved QSW VRM		
			300kHz	1 MHz	10MHz
LDDMOS	10	77	95%	91%	88%
Today's Device	30	473	87%	79%	60%

V. OTHER POWER MANAGEMENT ISSUES

A. *Advanced system architecture*

Today's VRM is powered up from the voltages that already exist that are used for supplying various parts of the system, for example, disk drives (12-V or 5-V) or the logic circuits operating from higher voltage (5-V). The future VRM is required to provide lower voltage and higher current with tighter voltage regulation. The traditional centralized power system will no longer meet the stringent requirements for voltage regulation because of the distributed impedance associated with a long power bus and

the parasitic ringing due to high-frequency operation. For future microprocessor applications, a Distributed Power System (DPS) must be developed. With a DPS system, VRM can be located very close to the processor.

Figure 20 shows a distributed power system. DPS has gained rapid acceptance in computer in recent years. The benefits of DPS includes flexibility, point-to-load regulation with precise control, the ability to integrate the converter with processor, increased reliability with N+1 redundancy at low cost, and parallel operation for wide range high-current, high-power applications. The standard used DPS design will also provide relatively short design cycles with a considerable advantage in marketing time which is critical for the rapidly evolving technologies and applications in the field of computer and communications.

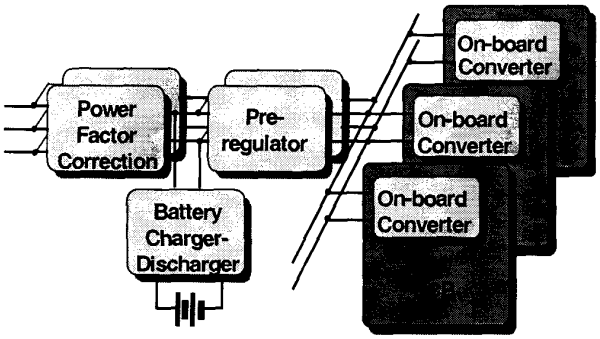


Fig. 20 Typical Distributed Power System

B. Advanced integration packaging technology

While novel topologies can partially alleviate the problems facing the future generation VRMs, the parasitic inductance due to circuit interconnections still posts the fundamental limitation in its ability to regulate the output voltage under load transients. To minimize the effect of the interconnection, an innovation design with possible integration of VRM and the processor is key to meet the ever increasing demand of processor performance and speed.

The integration of VRM with processor can take either a hybrid or monolithic approach. In the hybrid approach, the VRM can be made as a silicon chip with all the control functions. Figure 21 shows an integration-packaging example. As shown in Figure 21 (a) and (b), several VRM chips can be put in parallel and be mounted close to the microprocessor in the same cartridge. Ceramic capacitors with small ESR and ESL can be used as the output capacitors and be placed on the PCB board next to the processor. By connecting the output of the VRM and the power input of the processor via a path through a magnetic material sheet, the small output inductor can also be achieved. With this kind of packaging approach, interconnection parasitics can be minimized.

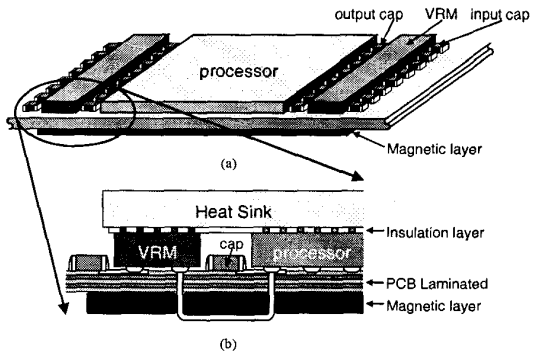


Fig. 21 Hybrid approach a) 3-D view and b) Side view

VI. Conclusion

For future microprocessor applications, there are many power management issues that need to be overcome, such as VRM topologies, power system architecture and packaging technologies. Among these important issues, the technical barrier is in today's power device technology. With newer device technology, VRM can be very cost effective, much faster and more efficient with very high power density.

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