# AN-366

Fairchild Semiconductor
Application Note
July 1984
Revised May 2001

FAIRCHILD SEMICONDUCTOR™

# Designer's Encyclopedia of One-Shots

## Introduction

Fairchild Semiconductor manufactures a broad variety of monostable multivibrators (one-shots) in bipolar and CMOS technologies. These products meet the stringent design needs in applications such as pulse generation, pulse shaping, time delay, demodulation, and edge detection of waveforms. Features of the various device types include single and dual monostable parts, retriggerable and non-retriggerable devices, direct clearing input, and DC or pulse-triggered inputs. To provide the designer with complete flexibility in controlling the pulse width, some devices also have Schmitt Trigger input, and/or contain internal timing components for added design convenience.

## Description

One-shots are versatile devices in digital circuit design. They are actually quite easy to use and are best suited for applications to generate or to modify short timings ranging from several tens of nanoseconds to a few microseconds. However, difficulties are constantly being experienced by design and test engineers. Generally, problems fall into the categories of either pulse width or triggering difficulties.

The purpose of this note is to present an overview of what one-shots are, how they work, and how to use them properly. It is intended to give the reader comprehensive information which will serve as a designer's guide to one-shots.

Nearly all malfunctions and failures on one-shots are caused by misuse or misunderstanding of their fundamental operating rules, characteristic design equations, parameters, or more frequently by poor circuit layout, improper by-passing, and improper triggering signal.

In the following sections all one-shots (bipolar and MOS) manufactured by Fairchild Semiconductor are presented with features tables and design charts for comparisons. Operating rules are outlined for devices in general and for specific device types. Notes on unique differences per device and on special operating considerations are detailed. Also included is a PC layout of a one-shot AC test adapter board and typical one-shot applications. Finally, truth tables and connection diagrams are included for reference.

## Definition

A one-shot integrated circuit is a device that, when triggered, produces an output pulse width that is independent of the input pulse width, and can be programmed by an external Resistor-Capacitor (RC) network. The output pulse width will be a function of the RC time constant. There are various one-shots manufactured by Fairchild Semiconductor that have diverse features, although, all one-shots have the basic property of producing a programmable output pulse width. All Fairchild one-shots have True and Complementary outputs, and both positive and negative edge-triggered inputs.

## Bipolar One-Shot Features

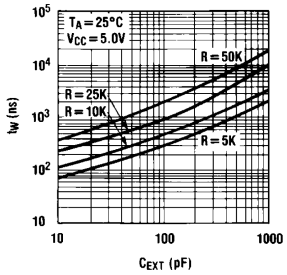
| Device Number | Number of One-Shots per IC Package | Re-Trigger | Reset | Capacitor | | Resistor | | Timing Equation (Note 1) for CEXT ≫ 1000 pF |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| | | | | μF | | kΩ | | |
| DM74121 | One | No | No | 0 | 1000 | 1.4 | 40 | $t_W = KRC \bullet (1 + 0.7 / R)$, $K \approx 0.7$ |
| DM74LS122 | One | Yes | Yes | None | | 5 | 260 | $t_W = KRC$, $K \approx 0.37$ |
| DM74123 | Two | Yes | Yes | None | | 5 | 50 | $t_W = KRC \bullet (1 + 0.7 / R)$, $K \approx 0.34$ |
| DM74LS123 | Two | Yes | Yes | None | | 5 | 260 | $t_W = KRC$, $K \approx 0.37$ |
| DM74LS221 | Two | No | Yes | 0 | 1000 | 1.4 | 100 | $t_W = KRC$, $K \approx 0.7$ |
| DM9601 | One | Yes | No | None | | 5 | 50 | $t_W = KRC \bullet (1 + 0.7 / R)$, $K \approx 0.34$ |
| DM9602 | Two | Yes | Yes | None | | 5 | 50 | $t_W = KRC \bullet (1 + 1 / R)$, $K \approx 0.34$ |

**Note 1:** The timing equations hold for all combinations of $R_{EXT}$ and $C_{EXT}$ for all cases of $C_{EXT} > 1000$ pF within specified limits on the $R_{EXT}$ and $C_{EXT}$. "K" can be treated as an invariant for $C_{EXT} \gg 1000$ pF. Refer to "K" vs. $C_{EXT}$ curves.

## Typical Output Pulse Width vs. Timing Components

Timing equations listed in the features tables hold for all combinations of $R_{EXT}$ and $C_{EXT}$ for all cases of $C_{EXT} > 1000$ pF. For cases where the $C_{EXT} < 1000$ pF, use the graphs shown below.

**DM9602**

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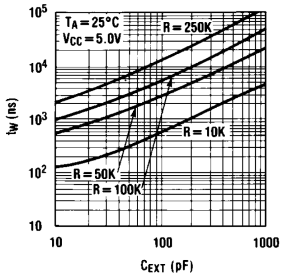


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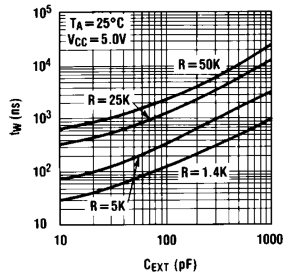


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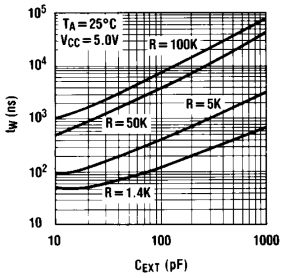


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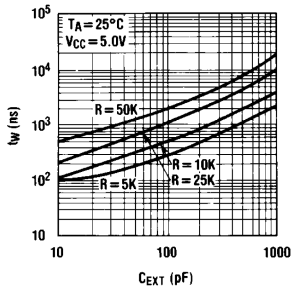

## Typical Output Pulse Width Variation vs. Ambient Temperature

The graphs shown below demonstrate the typical shift in the device output pulse widths as a function of temperature. It should be noted that these graphs represent the temperature shift of the device after being corrected for any temperature shift in the timing components. Any shift in these components will result in a corresponding shift in the pulse width, as well as any shift due to the device itself.

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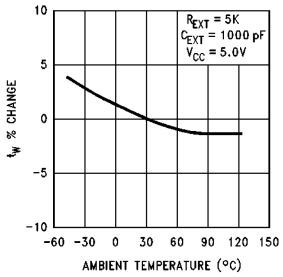


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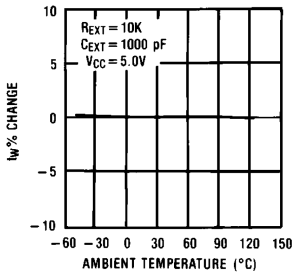


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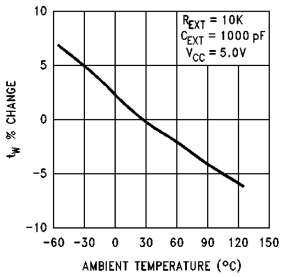


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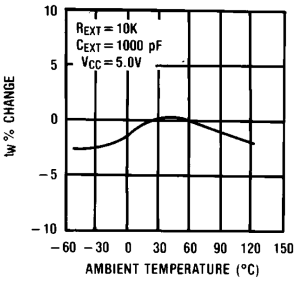


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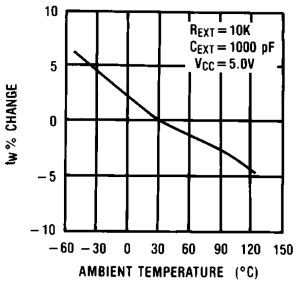
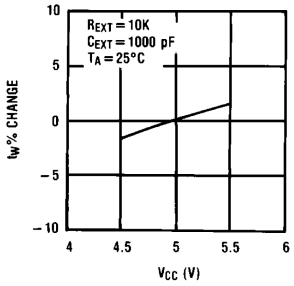


## Typical Output Pulse Width Variation vs. Supply Voltage

The following graphs show the dependence of the pulse width on $V_{CC}$.

As with any IC applications, the device should be properly bypassed so that large transient switching currents can be easily supplied by the bypass capacitor. Capacitor values of 0.001 to 0.10 µF are generally used for the $V_{CC}$ bypass capacitor.

**DM9602**

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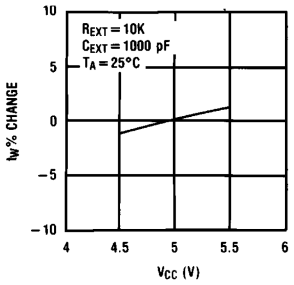


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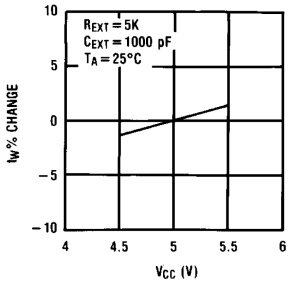


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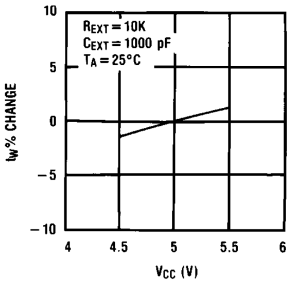


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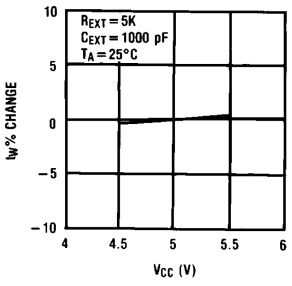
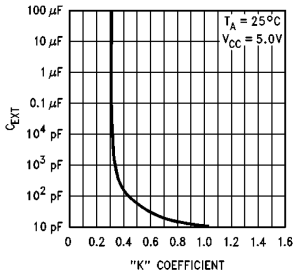


## Typical “K” Coefficient Variation vs. Timing Capacitance

For certain one-shots, the “K” coefficient is not a constant, but varies as a function of the timing capacitor $C_{EXT}$. The graphs below detail this characteristic.

**DM9602**

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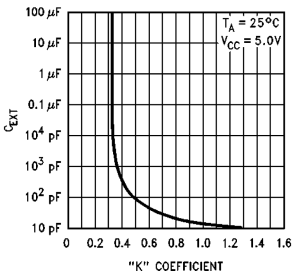


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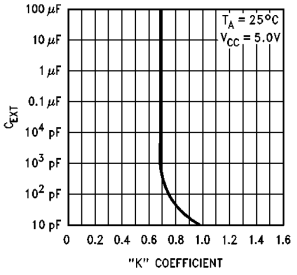


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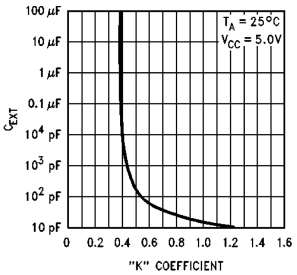


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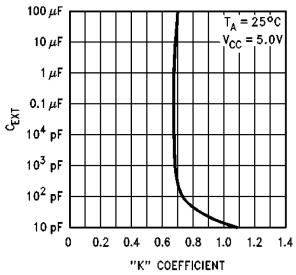
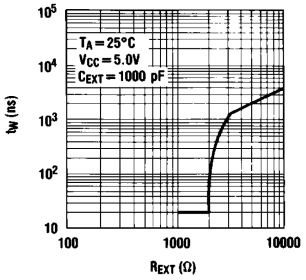


## Typical Output Pulse Width vs. Minimum Timing Resistance

The plots shown below demonstrate typical pulse widths and limiting values of the true output as a function of the external timing resistor, $R_{EXT}$. This information should alleviate concerns about operating one-shots with lower than recommended minimum $R_{EXT}$ values.

**DM9602**

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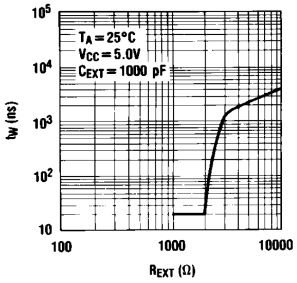


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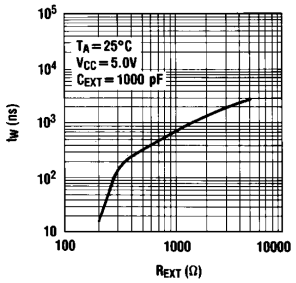


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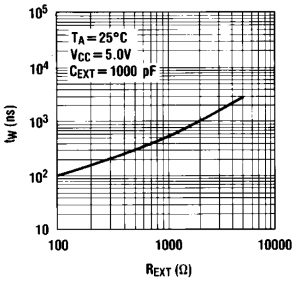


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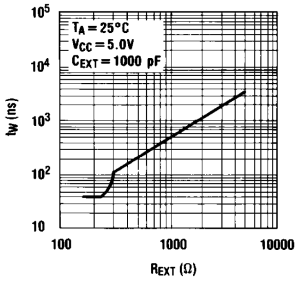


## Truth Tables

**74121**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| A1 | A2 | B | Q | $\overline{Q}$ |
| L | X | H | L | H |
| X | L | H | L | H |
| X | X | L | L | H |
| H | H | X | L | H |
| H | ↓ | H | ⎍ | ⎎ |
| ↓ | H | H | ⎍ | ⎎ |
| ↓ | ↓ | H | ⎍ | ⎎ |
| L | X | ↑ | ⎍ | ⎎ |
| X | L | ↑ | ⎍ | ⎎ |

**74123, 74L123A**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| A | B | CLR | Q | $\overline{Q}$ |
| H | X | H | L | H |
| X | L | H | L | H |
| L | ↑ | H | ⎍ | ⎎ |
| ↓ | H | H | ⎍ | ⎎ |
| X | X | L | L | H |

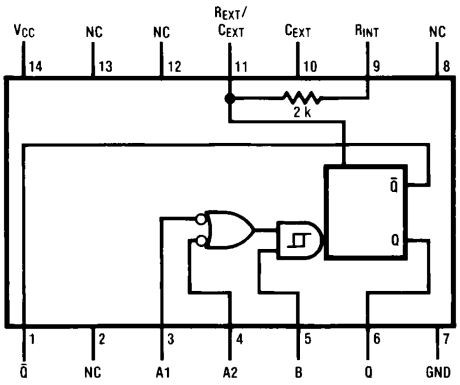
**74LS123**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | A | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⎍ | ⎎ |
| H | ↓ | H | ⎍ | ⎎ |
| ↑ | L | H | ⎍ | ⎎ |

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

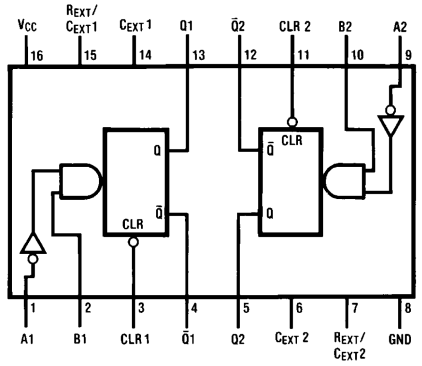
## Connection Diagrams

**74121**



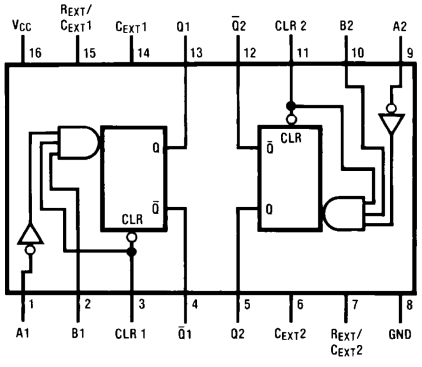

**Top View**

**74123, 74L123A**




**Top View**

**74LS123**




**Top View**

## Truth Tables (Continued)

**9602**

| Pin Numbers | | | Operation |
|---|---|---|---|
| A | B | CLR | |
| H→L | L | H | Trigger |
| H | L→H | H | Trigger |
| X | X | L | Reset |

**74LS221**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | A | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⎍ | ⎌ |
| H | ↓ | H | ⎍ | ⎌ |
| ↑ | L | H | ⎍ | ⎌ |

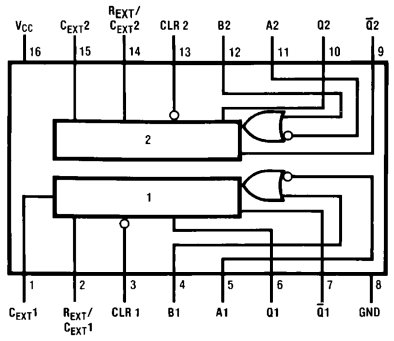
**9601**

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| A1 | A2 | B1 | B2 | Q | $\overline{Q}$ |
| H | H | X | X | L | H |
| X | X | L | X | L | H |
| X | X | X | L | L | H |
| L | X | H | H | L | H |
| L | X | ↑ | H | ⎍ | ⎌ |
| L | X | H | ↑ | ⎍ | ⎌ |
| X | L | H | H | L | H |
| X | L | ↑ | H | ⎍ | ⎌ |
| X | L | H | ↑ | ⎍ | ⎌ |
| H | ↓ | H | H | ⎍ | ⎌ |
| ↓ | ↓ | H | H | ⎍ | ⎌ |
| ↓ | H | H | H | ⎍ | ⎌ |

H = HIGH Level  L = LOW Level  X = Don't Care
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎌ = One LOW Level Pulse

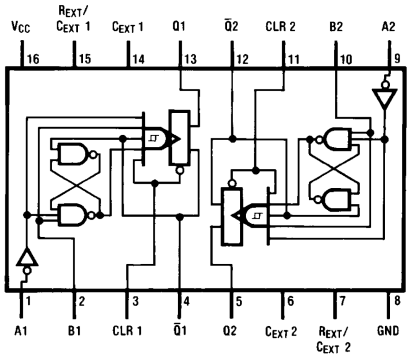
## Connection Diagrams (Continued)

**9602**



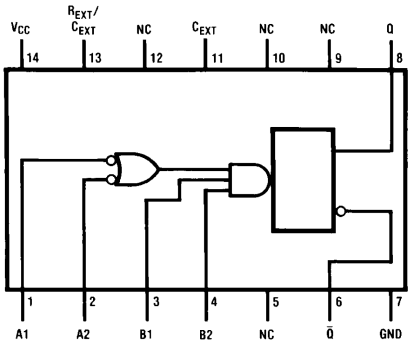

**Top View**

**74LS221**




**Top View**

**9601**




**Top View**

## CMOS One-Shot Features

| Device Number | Number of One-Shots per IC Package | Re-Trigger | Reset | Capacitor | | Resistor | | Timing Equation for $C_{EXT} > 1000$ pF |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| | | | | μF | | kΩ | | |
| MM74HC123 | Two | Yes | Yes | None | | 2 | (Note 2) | $t_W = RC$ |
| MM74C221 | Two | No | Yes | None | | 5 | (Note 2) | $t_W = RC$ |
| MM74HC221 | Two | No | Yes | None | | 2 | (Note 2) | $t_W = RC$ |
| MM74HC423 | Two | Yes | Yes | None | | 2 | (Note 2) | $t_W = RC$ |
| CD4528BC | Two | Yes | Yes | None | | 5 | (Note 2) | $t_W = 0.2\ RC\ In\ (V_{DD} - V_{SS})$ |
| CD4538BC | Two | Yes | Yes | None | | 5 | (Note 2) | $t_W = RC$ |
| MM74HC4538 | Two | Yes | Yes | None | | 1 | (Note 2) | $t_W = KRC, K \approx 0.74$ |
| CD4047BC | One | Yes | Yes | None | | 0.5 | (Note 2) | $t_W = KRC, K \approx 1.38$ |
| 74VHC123A | Two | Yes | Yes | None | | 5 | (Note 2) | $t_W = RC$ |
| 74VHC221A | Two | No | Yes | None | | 5 | (Note 2) | $t_W = RC$ |

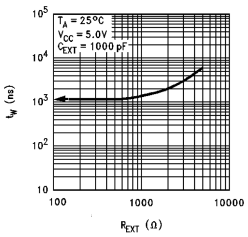
**Note 2:** Maximum usable resistance $R_X$ is a function of the leakage of the capacitance $C_X$ of the device, and leakage due to board layout, surface resistance, etc.

## Typical Output Pulse Width vs. Minimum Timing Resistance

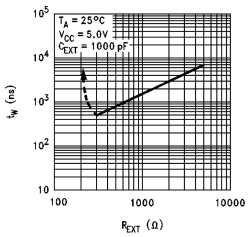
The plots shown demonstrate typical pulse widths and limiting values of the true output as a function of the external timing resistor, $R_{EXT}$. This information should alleviate concerns about operating one-shots with lower than recommended minimum $R_{EXT}$ values.

The arrow indicates the divergent point where timing resistor values beyond which results in outputs remaining indefinitely at a logic HIGH level.

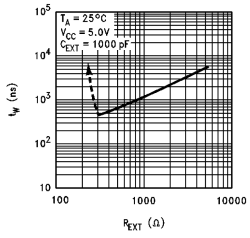
**MM74C221**



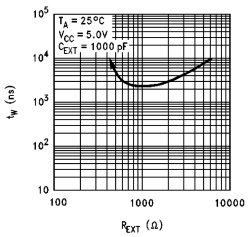

**MM74HC221**



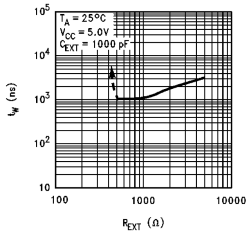

**MM74HC123**



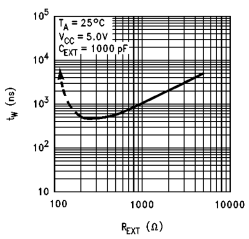

**MM14538, CD4538**




**MM14528, CD4528**




**MM74HC4538**



## Truth Tables

**MM74HC123, MM74HC221, 74VHC123A**

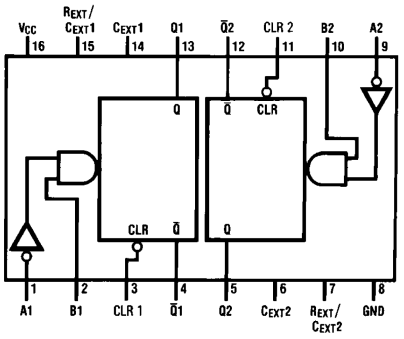
| Inputs | | | Outputs | |
|---|---|---|---|---|
| **Clear** | **A** | **B** | **Q** | $\overline{\mathbf{Q}}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⎍ | ⎎ |
| H | ↓ | H | ⎍ | ⎎ |
| ↑ | L | H | ⎍ | ⎎ |

**MM74HC423**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **Clear** | **A** | **B** | **Q** | $\overline{\mathbf{Q}}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⎍ | ⎎ |
| H | ↓ | H | ⎍ | ⎎ |

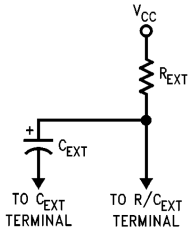
H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

## Connection Diagrams




**Top View**

**Timing Component**



## Truth Tables (Continued)

**MM74HC4538**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **Clear** | **A** | **B** | **Q** | $\overline{\mathbf{Q}}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⎍ | ⎎ |
| H | ↓ | H | ⎍ | ⎎ |
| H | ↑ | H | ⎍ | ⎎ |

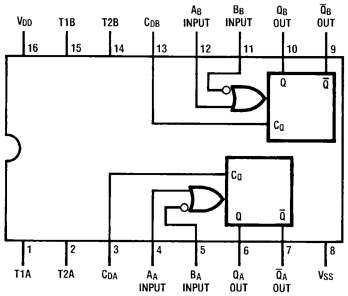
**MM74C221**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **Clear** | **A** | **B** | **Q** | $\overline{\mathbf{Q}}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⎍ | ⎎ |
| H | ↓ | H | ⎍ | ⎎ |

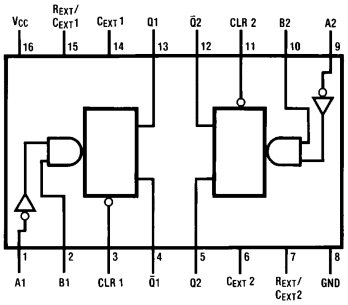
H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

## Connection Diagrams (Continued)

**MM74HC4538**

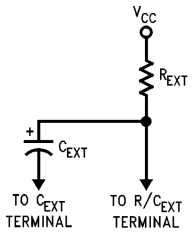



**MM74C221**



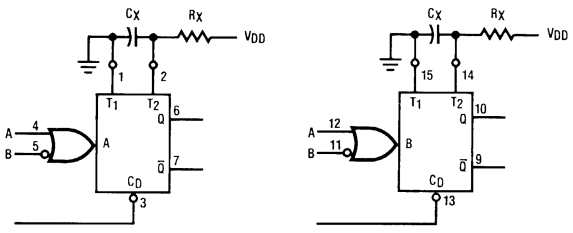

**Top View**

**Timing Component**




## Block Diagrams

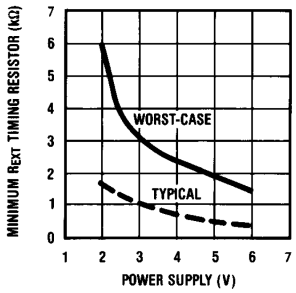
**$R_X$ and $C_X$ Are External Timing Components**



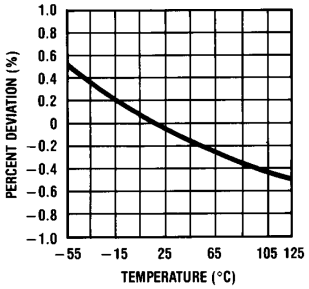
## Typical Performance Characteristics

**MM74HC123, MM74HC423, MM74HC221, MM74HC4538, 74VHC123A**

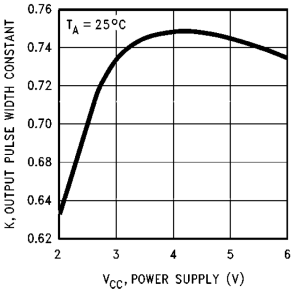
**Minimum $R_{EXT}$ vs. Supply Voltage**



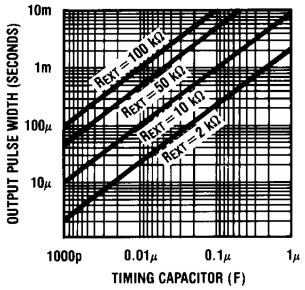

**Typical 1 ms Pulse Width Variation vs. Temperature**



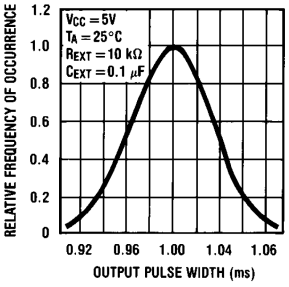

**Typical "K" Coefficient Variation vs. Supply Voltage MM74HC4538**



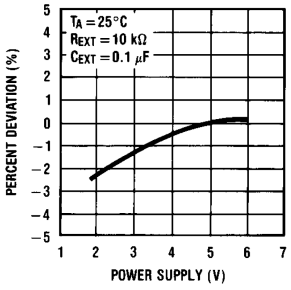

**Typical Output Pulse Width vs. Timing Components**




**Typical Distribution of Output Pulse Width, Part to Part**



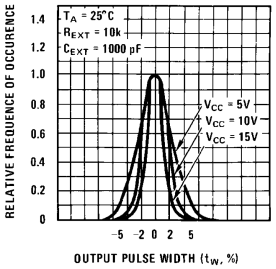

**Typical 1 ms Pulse Width Variation vs. Supply Voltage**



## Typical Performance Characteristics (Continued)

**MM74C221**

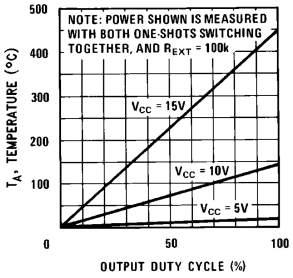
**Typical Distribution of Units for Output Pulse Width**



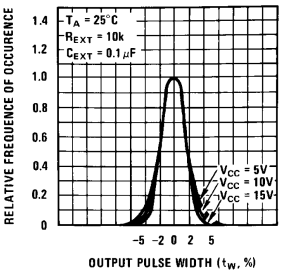

0% POINT PULSE WIDTH:
AT $V_{CC}$ = 5V, $t_W$ = 10.6 μs
AT $V_{CC}$ = 10V, $t_W$ = 10 μs
AT $V_{CC}$ = 15V, $t_W$ = 9.8 μs

PERCENTAGE OF UNITS WITHIN ±4%
AT $V_{CC}$ = 5V, 90% OF UNITS
AT $V_{CC}$ = 10V, 95% OF UNITS
AT $V_{CC}$ = 15V, 98% OF UNITS

**Typical Power Dissipation per Package**



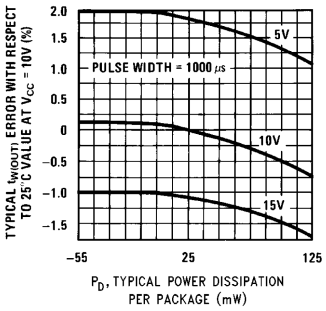

**Typical Distribution of Units for Output Pulse Width**



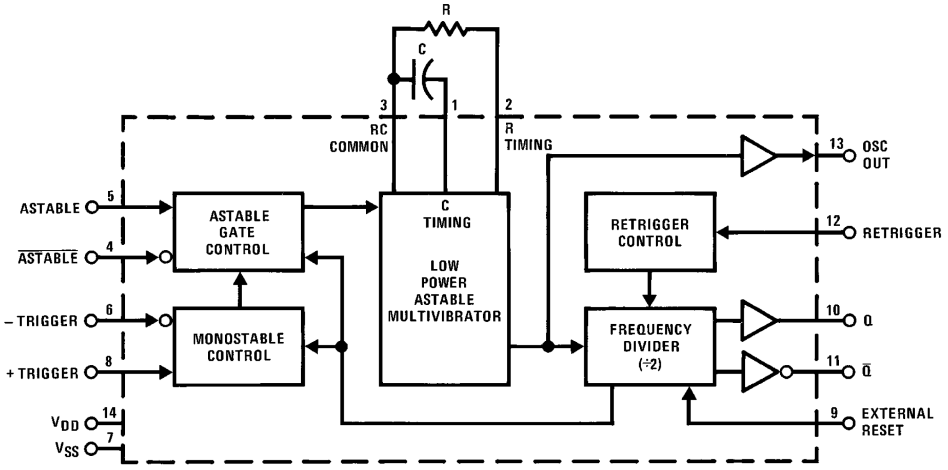

0% POINT PULSE WIDTH:
AT $V_{CC}$ = 5V, $t_W$ = 1020 μs
AT $V_{CC}$ = 10V, $t_W$ = 1000 μs
AT $V_{CC}$ = 15V, $t_W$ = 987 μs

PERCENTAGE OF UNITS WITHIN ±4%
AT $V_{CC}$ = 5V, 95% OF UNITS
AT $V_{CC}$ = 10V, 97% OF UNITS
AT $V_{CC}$ = 15V, 98% OF UNITS

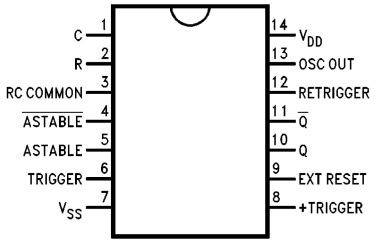
**Typical Variation in Output Pulse Width vs. Temperature**



## Block and Connection Diagrams
## CD4047BC




**Dual-In-Line and Flat Package**

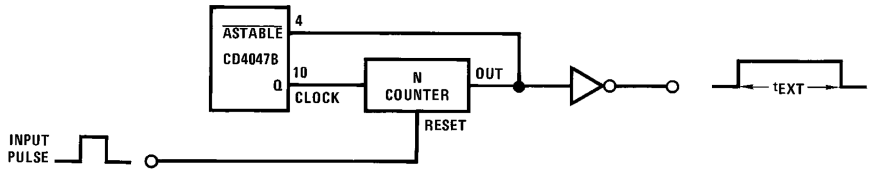



## Truth Table
## CD4047BC

| Function | Terminal Connections | | | Output Pulse From | Typical Output Period or Pulse Width |
|---|---|---|---|---|---|
| | To $V_{DD}$ | To $V_{SS}$ | Input Pulse To | | |
| Astable Multivibrator | | | | | |
| Free-Running | 4, 5, 6, 14 | 7, 8, 9, 12 | | 10, 11, 13 | |
| True Gating | 4, 6, 14 | 7, 8, 9, 12 | 5 | 10, 11, 13 | $t_A$ (10, 11) = 4.40 RC |
| Complement Gating | 6, 14 | 5, 7, 8, 9, 12 | 4 | 10, 11, 13 | $t_A$ (13) = 2.20 RC |
| Monostable Multivibrator | | | | | |
| Positive Edge-Trigger | 4, 14 | 5, 6, 7, 9, 12 | 8 | 10, 11 | |
| Negative Edge-Trigger | 4, 8, 14 | 5, 7, 9, 12 | 6 | 10, 11 | $t_M$ (10, 11) = 2.48 RC |
| Retriggerable | 4, 14 | 5, 6, 7, 9 | 8, 12 | 10, 11 | |
| External Countdown (Note 3) | 14 | 5, 6, 7, 8, 9, 12 | (see Figure 1) | (see Figure 1) | (see Figure 1) |

**Note 3:** External resistor between terminals 2 and 3; external capacitor between terminals 1 and 3.

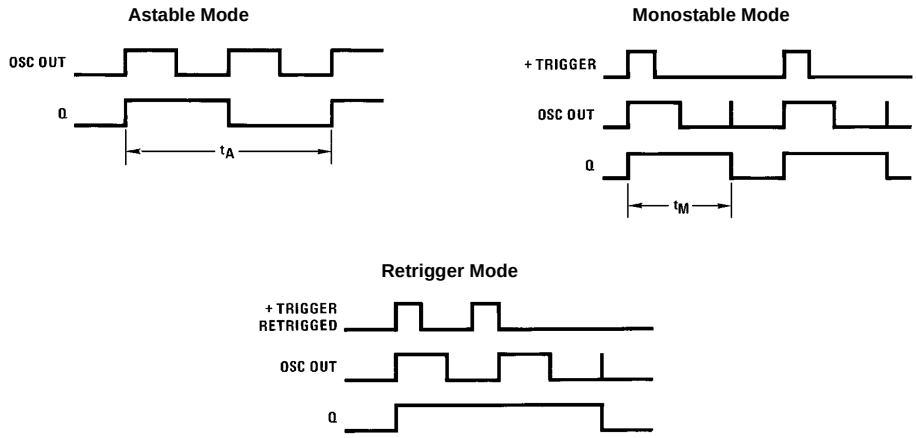
## Typical Implementation of External Countdown Option CD4047BC




$$t_{EXT} = (N-1)\,t_A + (t_M + t_A/2)$$

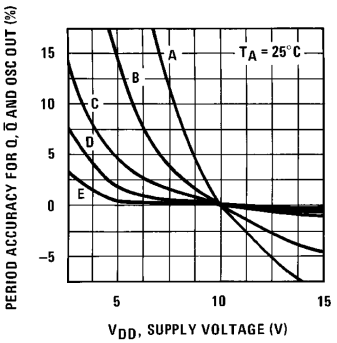
**FIGURE 1.**

## Timing Diagrams CD4047BC



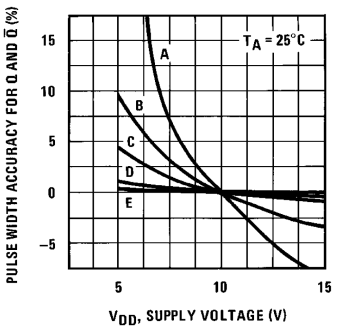
# Typical Performance Characteristics
# CD4047BC

**Typical Q, $\overline{Q}$, Osc Out Period Accuracy vs. Supply Voltage (Astable Mode Operation)**



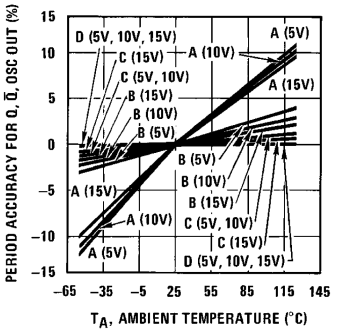

| | fQ, $\overline{Q}$ | R | C |
|---|---|---|---|
| **A** | 1000 kHz | 22 kΩ | 10 pF |
| **B** | 100 kHz | 22 kΩ | 100 pF |
| **C** | 10 kHz | 220 kΩ | 100 pF |
| **D** | 1 kHz | 220 kΩ | 1000 pF |
| **E** | 100 Hz | 2.2 MΩ | 1000 pF |

**Typical Q, $\overline{Q}$, Pulse Width Accuracy vs. Supply Voltage (Monostable Mode Operation)**



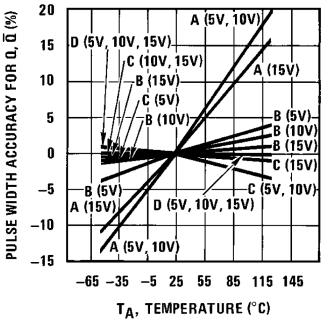

| | $t_M$ | R | C |
|---|---|---|---|
| **A** | 2 µs | 22 kΩ | 10 pF |
| **B** | 7 µs | 22 kΩ | 100 pF |
| **C** | 60 µs | 220 kΩ | 100 pF |
| **D** | 550 µs | 220 kΩ | 1000 pF |
| **E** | 5.5 ms | 2.2 MΩ | 1000 pF |

**Typical Q, $\overline{Q}$ and Osc Out Period Accuracy vs. Temperature (Astable Mode Operation)**




| | fQ, $\overline{Q}$ | R | C |
|---|---|---|---|
| **A** | 1000 kHz | 22 kΩ | 10 pF |
| **B** | 100 kHz | 22 kΩ | 100 pF |
| **C** | 10 kHz | 220 kΩ | 100 pF |
| **D** | 1 kHz | 220 kΩ | 1000 pF |

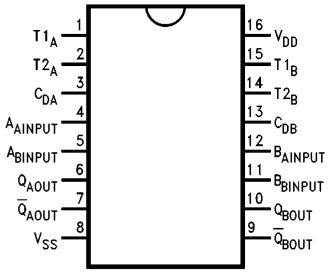
**Typical Q and $\overline{Q}$ Pulse Width Accuracy vs. Temperature (Monostable Mode Operation)**




| | $t_M$ | R | C |
|---|---|---|---|
| **A** | 2 µs | 22 kΩ | 10 pF |
| **B** | 7 µs | 22 kΩ | 100 pF |
| **C** | 60 µs | 220 kΩ | 100 pF |
| **D** | 500 µs | 220 kΩ | 1000 pF |

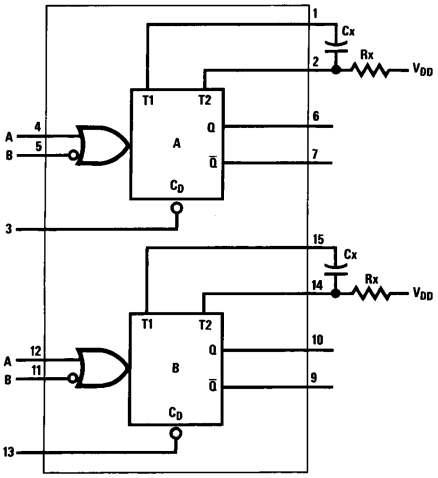
## Block and Connection Diagrams
## CD4528BC

**Dual-in-Line Package**




**Top View**

**Dual-in-Line Package**



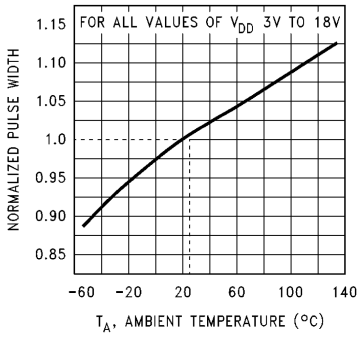

**Top View**

## Truth Table

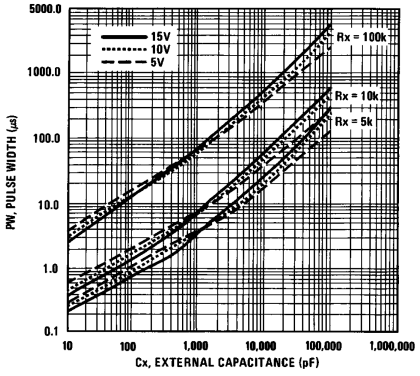
| Inputs | | | Outputs | |
|---|---|---|---|---|
| **Clear** | **A** | **B** | **Q** | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↓ | ⎍ | ⎎ |
| H | ↑ | H | ⎍ | ⎎ |

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

**Normalized Pulse Width vs. Temperature**




**Pulse Width vs. $C_X$**

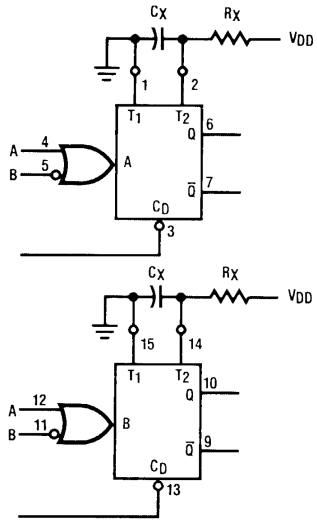


## Truth Table
## CD4538BC

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | A | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↓ | ⎍ | ⎍ |
| H | ↑ | H | ⎍ | ⎍ |

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎍ = One LOW Level Pulse
X = Don't Care

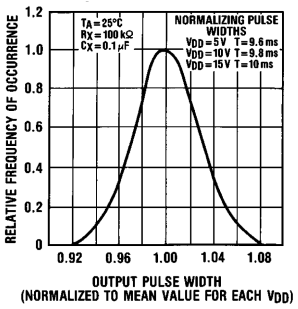
## Block Diagrams
## CD4538BC



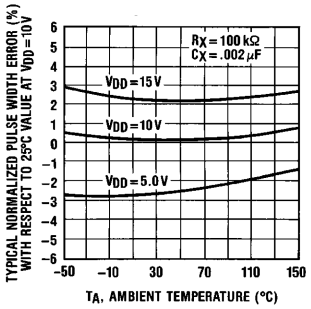

**$R_X$ and $C_X$ are External Components**
**$V_{DD}$ = Pin 16**
**$V_{SS}$ = Pin 8**

## Typical Performance Characteristics
## CD4538BC

**Typical Normalized Distribution of Units for Output Pulse Width**

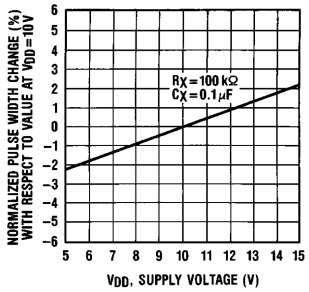



**Typical Pulse Width Error vs. Temperature**

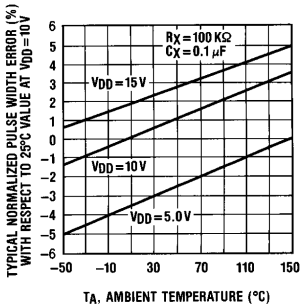


## Typical Performance Characteristics CD4538BC (Continued)

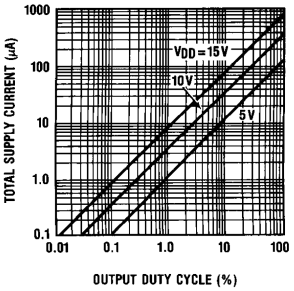
**Typical Pulse Width Variation as a Function of Supply Voltage $V_{DD}$**



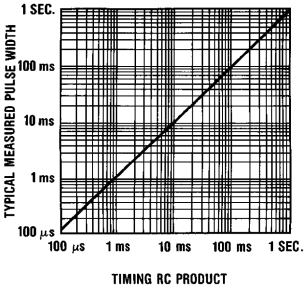

**Typical Pulse Width Error vs. Temperature**




**Typical Total Supply Current vs. Output Duty Cycle**
**$R_X$ = 100 kΩ, $C_L$ = 50 pF, $C_X$ = 100 pF**
**(One Monostable Switching Only)**




**Typical Pulse Width vs. Timing RC Product**



## Operating Rules

In all cases, R and C represented by the timing equations are the external resistor and capacitor, called $R_{EXT}$ and $C_{EXT}$, respectively, in the databook. All the foregoing timing equations use C in pF, R in KΩ, and yield, $t_W$, in nanoseconds. For those one-shots that are not retriggerable, there is a duty cycle specification associated with them that defines the maximum trigger frequency as a function of the external resistor, $R_{EXT}$.

In all cases, an external (or internal) timing resistor ($R_{EXT}$) connects from $V_{CC}$ or another voltage source to the "$R_{EXT}$/$C_{EXT}$" pin, and an external timing capacitor ($C_{EXT}$) connects between the "$R_{EXT}$/$C_{EXT}$" and "$C_{EXT}$" pins are required for proper operation. There are no other elements needed to program the output pulse width, though the value of the timing capacitor may vary from 0.0 to any necessary value.

When connecting the $R_{EXT}$ and $C_{EXT}$ timing elements, care must be taken to put these components as close to the device pins as possible, electrically and physically. Any distance between the timing components and the device will cause time-errors in the resulting pulse width. This is because the series impedance (both resistive and inductive) will result in a voltage difference between the capacitor and the one-shot. Since the one-shot is designed to discharge the capacitor to a specific fixed voltage, the series voltage will "fool" the one-shot into releasing the capacitor before the capacitor is fully discharged. This will result in a pulse width that appears much shorter than the programmed value. We have encountered users who have been frustrated by pulse width problems and had difficulty performing correlations with commercial test equipment. The nature of such problems is usually related to improper layout of the DUT adapter boards. See Figure 7 for a PC layout of an AC test adapter board. It has been demonstrated that lead length greater than 3 cm from the timing component to the device pins can cause pulse width problems on some devices.

For precise timing, precision resistors with good temperature coefficients should be used. Similarly, the timing capacitor must have low leakage, good dielectric absorption characteristic, and a low temperature coefficient for stability. Please consult manufacturers to obtain the proper type of component for the application. For small time constants, high-grade mica glass, polystyrene, polypropylene, or poly carbonate capacitor may be used. For large time constants, use a solid tantalum or special aluminum capacitor.

In general, if small timing capacitor has leakage approaching 100 nA or if the stray capacitance from either terminal to ground is greater than 50 pF, then the timing equations or design curves which predict the pulse width would not represent the programmed pulse width the device generates.

When an electrolytic capacitor is used for $C_{EXT}$, a switching diode is often suggested for standard TTL one-shots to prevent high inverse leakage current (Figure 2). In general, this switching diode is not required for LS-TTL, CMOS, and HCMOS devices; it is also not recommended with retriggerable applications.

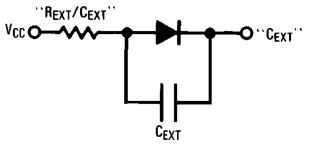



**FIGURE 2.**

It is never a good practice to leave any unused inputs of a logic integrated circuit "floating". This is particularly true for one-shots. Floating uncommitted inputs or attempts to establish a logic HIGH level in this manner will result in malfunction of some devices

Operating one-shots with values of the $R_{EXT}$ outside recommended limits is at the risk of the user. For some devices it will lead to complete functional failure, while for other devices it may result in either pulse widths different from those values predicted by design charts or equations, or with modes of operation and performance quite different from known standard characterizations.

To obtain variable pulse width by remote trimming, the following circuit is recommended (Figure 3). "Remote" should be placed as close to the one-shot as possible.

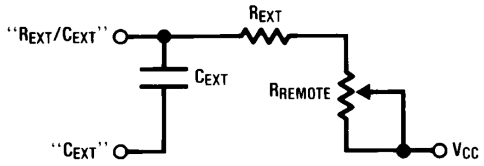
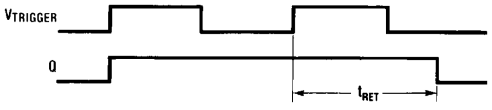



**FIGURE 3.**

$V_{CC}$ and ground wiring should conform to good high frequency standards and practices so that switching transients on the $V_{CC}$ and ground return leads do not cause interaction between one-shots. A 0.001 μF to 0.1 μF bypass capacitor (disk or monolithic type) from the $V_{CC}$ pin to ground is necessary on each device. Furthermore, the bypass capacitor should be located so as to provide as short an electrical path as possible between the $V_{CC}$ and ground pins. In severe cases of supply-line noise, decoupling in the form of a local power supply voltage regulator is necessary.

For retriggerable devices the retrigger pulse width is calculated as follows for positive-edge triggering:




$$t_{RET} = t_W + t_{PLH} = K \cdot (R_{EXT})(C_{EXT}) + t_{PHL}$$

**(See tables for exact expressions for K and $t_W$; K is unity on most HCMOS devices)**

**FIGURE 4.**

## Special Considerations and Notes

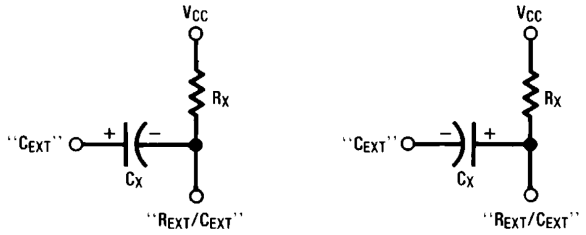
The 9601 is the single version of the dual 9602 one-shot. Except for the gating networks of the input sections, the timing circuitry of the 74VHC123A, MM74HC123, MM74HC221, MM74HC423, and MM74HC4538 are identical, and their performance characteristics are essentially the same. The design and characteristic curves for equivalent devices are not depicted individually, as they can be referenced from their parent device.

Fairchild's TTL-'123 dual retriggerable one-shot features a unique logic realization not implemented by other manufactureres. The "CLEAR" input does not trigger the device, a design tailored for applications where it is desired only to terminate or to reduce the timing pulse width.

The DM74LS221 and 74VHC221, even though they have pin-outs identical to the DM74LS123, are not functionally identical. It should be remembered that the '221 is a non-retriggerable one-shot, while the '123 is a retriggerable one. For the '123 devices, it is sometimes recommended to externally ground the "$C_{EXT}$" pin for improved system performance. The "$C_{EXT}$" pin on the '221, however, is not an internal connection to the device ground. Hence, grounding this pin on the '221 device will render the device inoperative.

Furthermore, if a polarized timing capacitor is used on the '221, the positive side of the capacitor should be connected to the "$C_{EXT}$" pin. For '123 parts, it is the contrary, the negative terminal of the capacitor should be connected to the "$C_{EXT}$" pin of the device. (Figure 5).

The '221 triggers on "CLEAR". This mode of trigger requires first the "B-Input" be set from a LOW-to-HIGH level while the "CLEAR" input is maintained at logic LOW level. With the "B" input at logic HIGH level, the "CLEAR" input positive transition from LOW-to-HIGH will trigger an output pulse ("A" input is LOW).




(74VHC221, DM74LS221) (74VHC123, DM74LS123)

**FIGURE 5.**

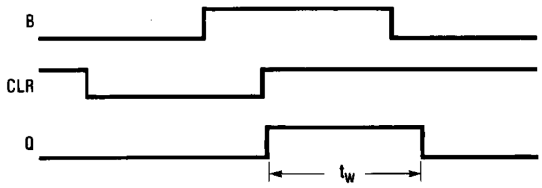



**FIGURE 6.**

## Special Considerations and Notes (Continued)

**AC Test Adapter Board**

The compact PC layout (Figure 7) is a universal one-shot test adapter board. By wiring different jumpers, it can be configured to accept all one-shots made by Fairchild Semiconductor. The configuration shown is dedicated for the '123 device. It has been used successfully for functional and pulse width testing on all the '123 families of one-shots on the Teradyne AC test system.

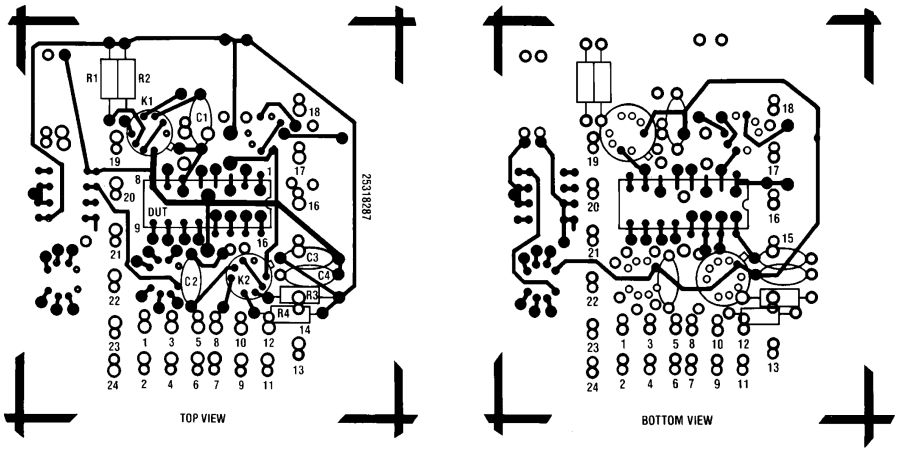
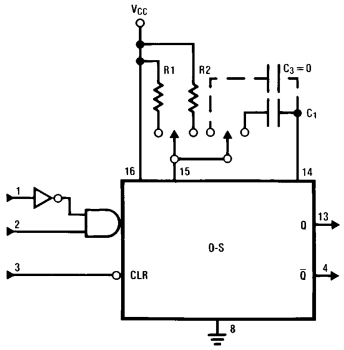


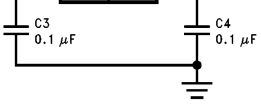

**FIGURE 7. AC Test Adapter**

**'123 One-Shot**

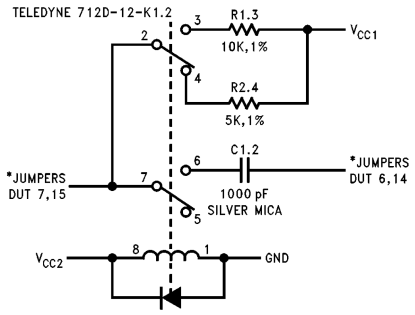



**Timing Components and I/O Connections to D.U.T.**

| DUT | CHAN |
|---|---|
| 1 | 6 |
| 2 | 5 |
| 3 | 4 |
| 4 | 22 |
| 5 | 23 |
| 6 | • |
| 7 | • |
| 8 | GND |
| 9 | 12 |
| 10 | 11 |
| 11 | 10 |
| 12 | 16 |
| 13 | 17 |
| 14 | • |
| 15 | • |
| 16 | $V_{CC1}$ |
| | $V_{CC2}$ |




**Typical Circuit**




**Note:** Textool 16 Pin DUT socket, do not use sockets for K1, 2.

**FIGURE 8.**

## Applications

The following circuits are shown with generalized one-shot connection diagram.

**Noise Discriminator (Figure 9)**

The time constant of the one-shot (O-S) can be adjusted so that an input pulse width narrower than that determined by the time constant will be rejected by the circuit. Output at $Q_2$ will follow the desired input pulse, with the leading edge delayed by the predetermined time constant. The output pulse width is also reduced by the amount of the time constant from $R_X$ and $C_X$.

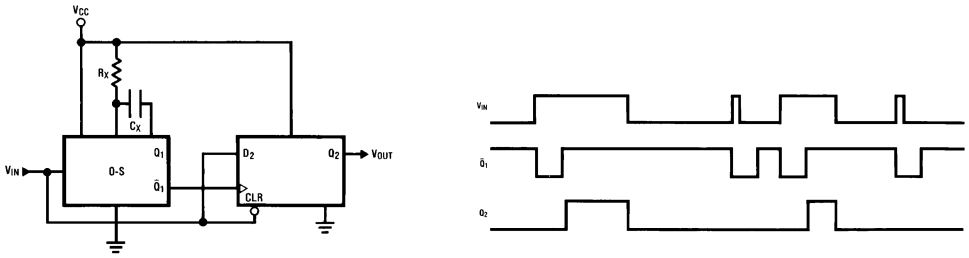



**FIGURE 9. Noise Discriminator**

**Frequency Discriminator (Figure 10)**

The circuit shown in Figure 10 can be used as a frequency-to-voltage converter. For a pulse train of varying frequency applied to the input, the one-shot will produce a pulse constant width for each triggering transition on its input. The output pulse train is integrated by $R_1$ and $C_1$ to yield a waveform whose amplitude is proportional to the input frequency. (Retriggerable device required.)

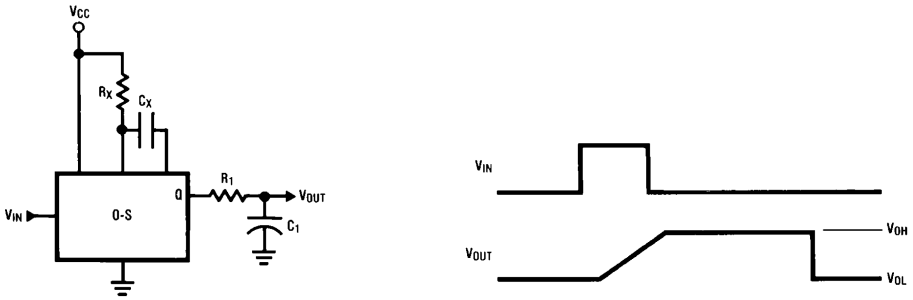



**FIGURE 10.**

## Applications (Continued)

**Envelope Detector (Figure 11)**

An envelope detector can be made by using the one-shot's retrigger mode. The time constant of the device is selected to be slightly longer than the period of each cycle within the input pulse burst. Two distinct DC levels are present at the output for the duration of the input pulse burst and for its absence (see Figure 11a). The same circuit can also be employed for a specific frequency input as a Schmitt Trigger to obviate input trigger problems associated with hysteresis and slow varying, noisy waveforms (see Figure 11b). (Retriggerable device required.)

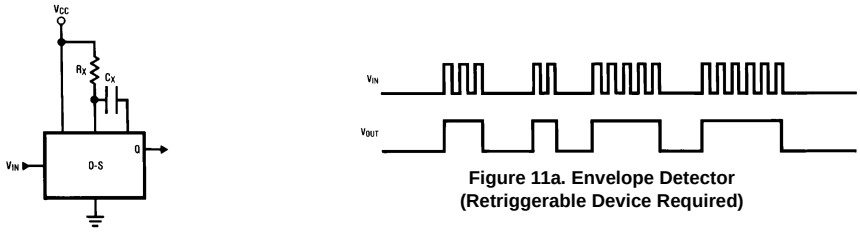



**Figure 11a. Envelope Detector (Retriggerable Device Required)**

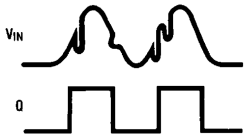
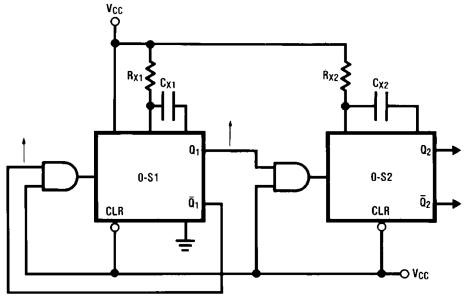


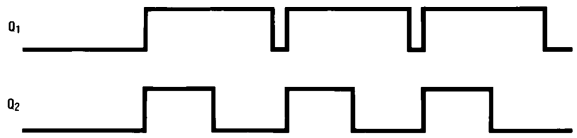

**Figure 11b. Schmitt Trigger**

**FIGURE 11.**

**Pulse Generator (Figure 12)**

Two one-shots can be connected together to form a pulse generator capable of variable frequency and independent duty cycle control. The $R_{X1}$ and $C_{X1}$ of O-S1 determine the frequency developed at output $Q_1$. $R_{X2}$ and $C_{X2}$ of O-S2 determine the output pulse width at $Q_2$. (Retriggerable device required.)




$$\text{DUTY CYCLE} = \frac{R_{X2}\,C_{X2}}{R_{X1}\,C_{X1}}$$

$$\text{FREQ} = \frac{1}{K\,R_{X1}\,C_{X1}}$$

**Note:** K is the multiplication factor dependent of the device. Arrow indicates edge-trigger mode.

**FIGURE 12. Pulse Generator (Retriggerable Device Required)**

## Applications (Continued)

**Delayed Pulse Generator with Override to Terminate Output Pulse (Figure 13)**

An input pulse of a particular width can be delayed with the circuit shown in Figure 13. Preselected values of $R_{X1}$ and $C_{X1}$ determine the delay time via O-S1, while preselected values of $R_{X1}$ and $C_{X2}$ determine the output pulse width through O-S2. The override input can additionally serve to modify the output pulse width.

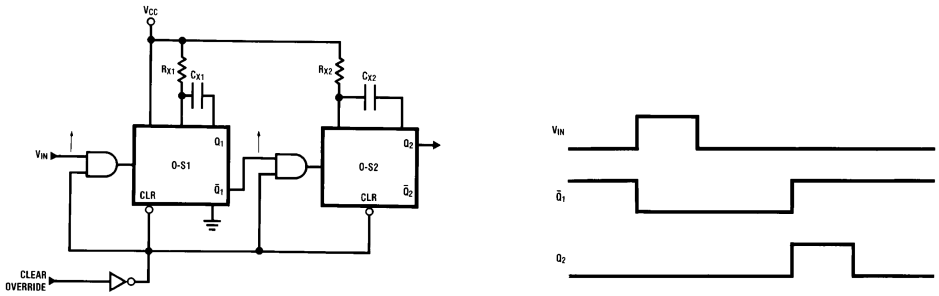



**FIGURE 13. Delayed Pulse Generator with Override to Terminate Output Pulse**

**Missing Pulse Detector (Figure 14)**

By setting the time constant of O-S1 through $R_{X1}$ and $C_{X1}$ to be at least one full period of the incoming pulse period, the one-shot will be continuously retriggered as long as no missing pulse occurs. Hence, $\overline{Q}_1$ remains LOW until a pulse is missing in the incoming pulse train, which then triggers O-S2 and produces an indicating pulse at $Q_2$. (Retriggerable device required.)

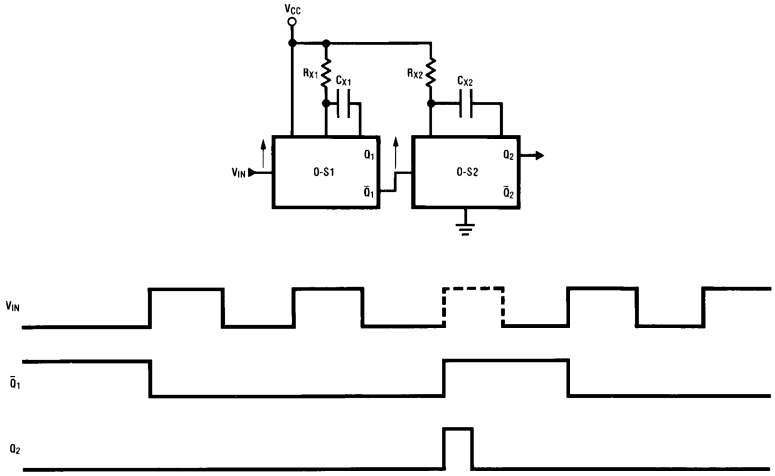



**FIGURE 14. Missing Pulse Detector (Retriggerable Device Required)**

## Applications (Continued)

**Pulse Width Detector (Figure 15)**

The circuit of Figure 15 produces an output pulse at $V_{OUT}$ if the pulse width at $V_{IN}$ is wider than the predetermined pulse width set by $R_X$ and $C_X$.

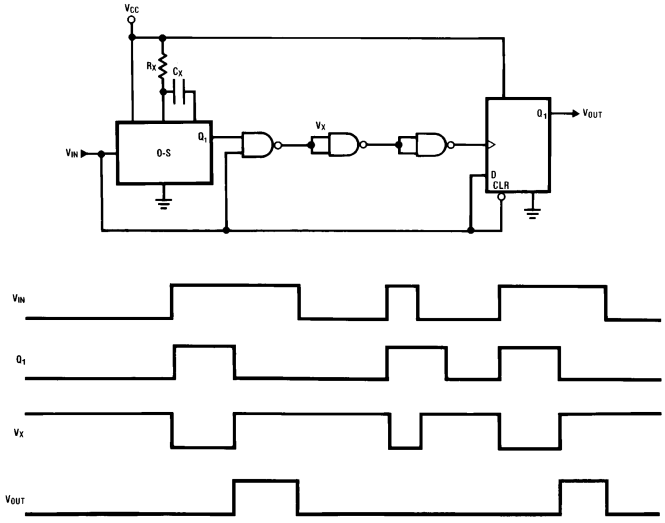



**FIGURE 15. Pulse Width Detector**

**Band Pass Filter (Figure 16)**

The band pass of the circuit is determined by the time constants of the two low-pass filters represented by O-S1 and O-S2. With the output at $Q_2$ delayed by C, the D-FF clocks HIGH only when the cutoff frequency of O-S2 has been exceeded. The output at $Q_3$ is gated with the delayed input pulse train at $Q_4$ to produce the desired output. (Retriggerable device required.)

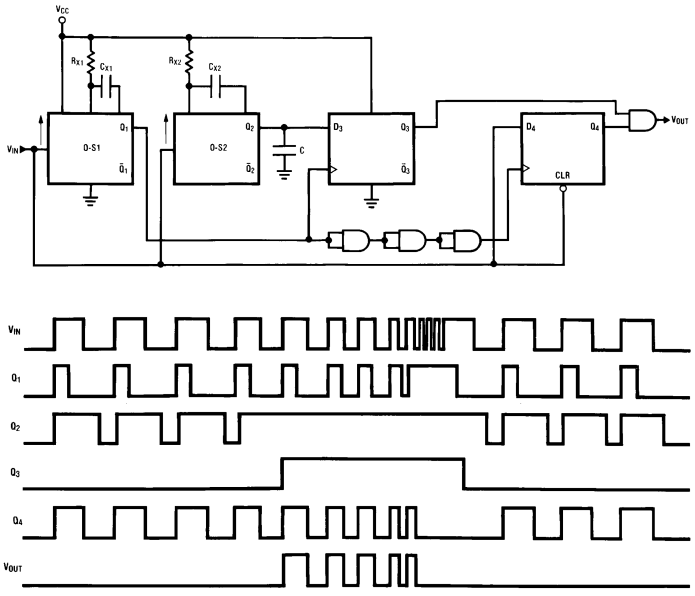



**FIGURE 16. Band Pass Filter (Retriggerable Device Required)**

## Applications (Continued)

**FM Data Separator (Figures 17, 18)**

The data separator shown in Figure 17 and Figure 18 is a two-time constant separator that can be used on tape and disc drive memory storage systems. The clock and data pulses must fall within pre-specified time windows. Both the clock and data windows are generated in this circuit. There are two data windows; the short window is used when the previous bit cell had a data pulse in it, while the long window is used when the previous bit cell had not data pulse.

If the data pulse initially falls into the data window, the −SEP DATA output returns to the NAND gate that generates the data window, to assure that the full data is allowed through before the window times out. The clock windows will take up the remainder of the bit cell time.

Assume all one-shots and flip-flops are reset initially and the +READ DATA has the data stream as indicated. With O-S1 and O-S2 inactive, +CLK WINDOW is active. The first +READ DATA pulse will be gated through the second AND gate, which becomes −SEP CLK for triggering of the R-S FF and the one-shots. With the D-FF off, O-S1 will remain reset. The −SEP CLK pulse will trigger O-S2, whose output is sent to the OR gate, and its output becomes +DATA WINDOW to enable the first AND gate. The next pulse on +READ DATA will be allowed through the first AND gate to become −SEP DATA. This pulse sets the R-S FF, whose HIGH output becomes the data to the D-FF. The D-FF is clocked on by O-S2 timing out and +CLK WINDOW becoming active. $\overline{Q_4}$ will hold O-S2 reset and allow O-S1 to trigger on the next clock pulse.

The next clock pulse (the second bit cell) is ANDed with +CLK WINDOW and becomes the next −SEP CLK, which will reset the R-S FF and trigger O-S1. As O-S1 becomes active, the +DATA WINDOW becomes active, enabling the first AND gate. With no data bit in the second bit cell, the R-S FF will remain reset, enabling the D-FF to be clocked off when +DATA WINDOW falls. When the D-FF is clocked off, $Q_4$ will hold O-S1 reset and allow O-S2 to be triggered.

The third clock pulse (bit cell 3) is ANDed with +CLK WINDOW and become −SEP CLK, which continues resetting the R-S FF and triggers O-S2. When O-S2 becomes active, +DATA WINDOW enables the first AND gate, allowing the data pulse in bit cell 3 to become −SEP DATA. This −SEP DATA will set the R-S FF, which enables the D-FF to be clocked on when +DATA WINDOW falls. When this happens, $Q_4$ will hold O-S2 reset and allow O-S1 to trigger. This procedure continues as long as there is clock and data pulse stream present on the +READ DATA line.

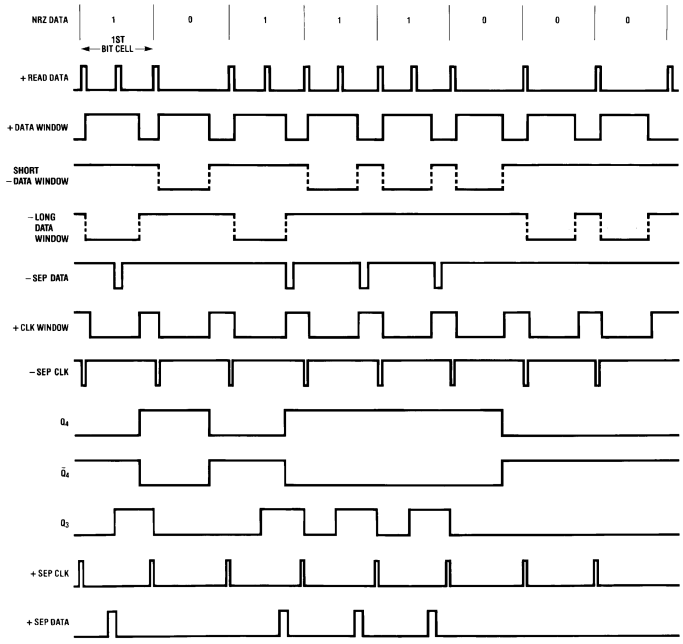



**FIGURE 17.**

## Applications (Continued)

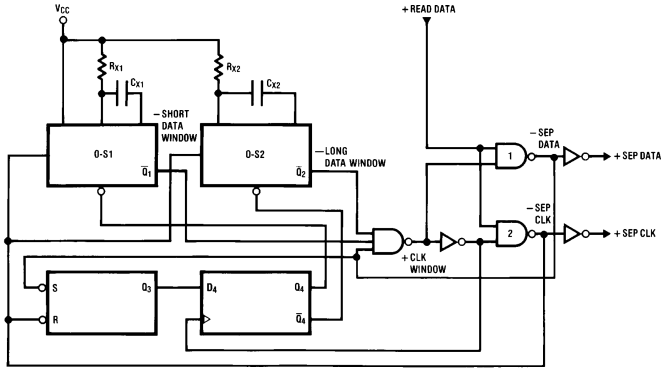



**FIGURE 18.**

**Phase-Locked Loop VCO (Figures 19, 20)**

The circuit shown in Figure 19 and Figure 20 represents the VCO in the data separation part of a rotational memory storage system which generates the bit rate synchronous clocks for write data timing and for establishing the read data windows.

The op-amp that preforms the phase-lock control operates by having its inverting input be driven by two sources that normally buck one another. One source is the one-shot, the other source is the phase detector flip-flop. When set, the one-shot, through an inverter, supplies a HIGH-level voltage to the summing node of the op-amp and the phase detector FF, also through an inverter, supplies a cancelling LOW-level input.

It is only when the two sources are out of phase with each other, that is one HIGH and the other LOW, that a positive- or negative-going phase error will be applied to the op-amp to effect a change in the VCO frequency. Figure 20 and Figure 20 illustrate the process of phase-error detection and correction when synchronizing to a data bit pattern. The rising edge of each pulse at DATA+PLO clocks the one-shot LOW and the phase detector FF HIGH. Since both outputs are still bucking each other, no change will be observed at the phase-error summing node. When the one-shot times out, if this occurs after the 2F clock has reset the phase detector FF to a LOW output, a positive pulse will be seen at the summing node until both the one-shot and the FF are reset. Any positive pulse will be reflected by a negative change in the op-amp output, which is integrated and reduces the positive voltage at the VCO input in direct proportion to the duration of the phase-error pulse. A negative phase-error pulse occurs when the phase detector FF remains set longer than the one-shot.

Negative phase-error pulse causes the integrated control voltage to swing positive in direct proportion to the duration of the phase-error pulse. It is recommended that a clamping circuit be connected to the output of the op-amp to prevent the VCO control voltage from going negative or more positive than necessary. A back-to-back diode pair connected between the op-amp and the VCO is highly recommended, for it will present a high impedance to the VCO input during locked mode. This way, stable and smooth operation of the PLO circuit is assured.

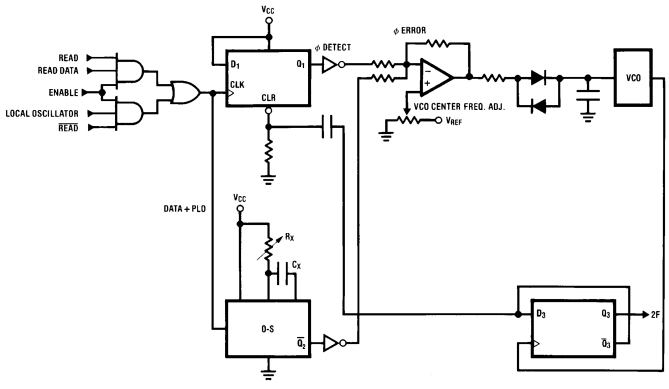



**FIGURE 19. 2F Bit Rate Synchronous Read/Write Clock**

## Applications (Continued)

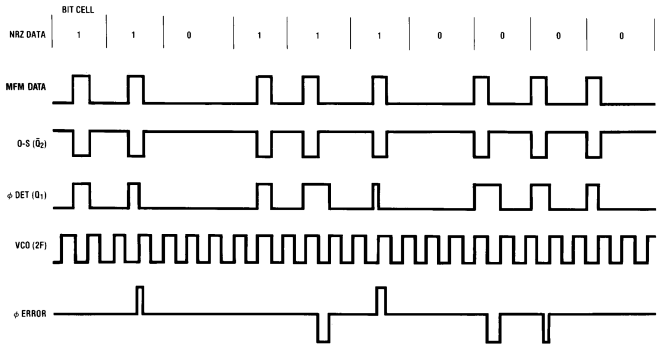



**FIGURE 20. Phase-Locked Loop Voltage Controlled Oscillator**

## A Final Note

It is hoped that this application note will clarify many pertinent and subtle points on the use and testing of one-shots. We invite your comments to this application note and solicit your constructive criticism to help us improve our service to you. Please email **logic.support@fairchildsemi.com**.