Measuring IC and ASIC Design Productivity

White Paper

Developed by
Numetrics Management Systems
5201 Great America Parkway, Suite 320
Santa Clara, CA 95054

Phone: (408) 562-5750
Fax: (408) 562-5712
Email: info@numetrics.com
Web Site: www.numetrics.com

May 2000

Overview on Measuring Design Productivity

I. Introduction

Maximizing IC design productivity has become critical to semiconductor and systems companies in the electronics industry. The capability to rapidly design complex, multi-million gate chips equates to tremendous competitive advantage, and high design productivity is the enabler.

Furthermore, the availability of manufacturing services from dedicated silicon foundries has sparked a trend toward outsourcing of chip manufacturing, which in turn has leveled the playing field between semiconductor companies that have fabs and those that do not. Owning a fab no longer offers the competitive advantage it once did, as fabless chip houses have just as much access to leading-edge fabrication technology as vertically integrated device manufacturers (IDMs). Design capability is now the key differentiator.

As semiconductor companies strengthen their design capabilities and broaden their product portfolios, systems companies must also distinguish their products from those comprising the off-the-shelf chips sold by semiconductor vendors. Systems manufacturers must therefore design ASICs that are even more advanced than those of semiconductor companies in order to achieve competitive differentiation. The need to boost design productivity has never been as important to systems companies as it is today.

Engineering resource shortages exacerbate the productivity improvement challenges facing both semiconductor and systems players. It's forcing them to increase design output and, hence, productivity of their existing engineering workforces.

In sum, design productivity is emerging as a key area of differentiation and competitive advantage among companies competing in the electronics industry. World-class design productivity equates to world class time-to-market capability.

Central to improving design productivity is measuring it, which is the reason why leading edge electronics companies have aggressively begun benchmarking themselves during the past 12 to 24 months.

II. Defining Design Productivity

What's the definition of design productivity? First we need to explore the definition of productivity (P) in general, which is defined as "output produced" divided by the "labor expended" on producing that output.

This yields a metric whose dimensions are "output per unit of labor input", where a unit of labor, for example, could be a worker-hour.

The equation for productivity (P) is as follows:

P = Output ÷ Labor Expended

If, for example, we apply this definition to manufacturing productivity (MP), we get the following:

MP = Value-added ÷ Labor Expended, or "value-added per worker-hour"

Where value-added is defined as follows:

Value-added ($) = (End product's selling price) – (Cost of materials of the product)

The resulting definition of MP is "dollars per worker-hour".

We would like to apply a similar definition to chip design productivity. If we do, the denominator remains the same, engineering effort expended, but what is the numerator? That is, what is the output of a chip design team? What does it produce? Certainly it produces circuitry in the form of transistors and gates, but neither transistor count nor gate count accurately reflects differences in design complexity from one chip to another.

As a simple example, consider that analog circuits typically are more complex than digital circuits and, therefore, demand much more engineering effort to create. A 100,000-transistor chip comprising 95% analog circuits typically requires much more design effort than a 100,000-transistor chip comprising 95% digital circuits. This is indeed the case. **Figure 1** (on the next page) shows that there is little correlation between transistor count and the amount of effort expended on designing a chip. Many high transistor count designs require significantly less effort than many small designs. So a productivity metric whose dimensions are "transistors per engineer-hour" or "gates per engineer-hour" is not an accurate measure.

Instead, we need a unit of designer output that accurately reflects chip complexity. Complexity refers to "difficulty of design" or rather the amount of engineering effort required to design a chip. It's axiomatic that the more complex a design is, the more effort it demands. So when we say that one design is "more complex" than another, we're implying that one design requires more engineering effort than another does.

If, for example, we could say conclusively that one chip's complexity is ten thousand "complexity units" and another chip's is five thousand "complexity units," then the former would require twice as much effort and therefore would be exactly twice as "complex" as the latter.

We then could divide the respective complexities of each chip by the particular amount of design effort expended on each, and this would yield an accurate measure of productivity (*e.g.* "complexity units per engineer-hour"). This of course is in sharp contrast to saying that one design has 10,000 transistors and another's is 5,000; for the former is not necessarily and, not at all likely to be, twice as complex as the latter.

Accurately quantifying complexity provides a gauge of what each design team truly produces and sets the stage for measuring productivity, because it enables us to make fair comparisons among different teams developing chips of varying complexity.

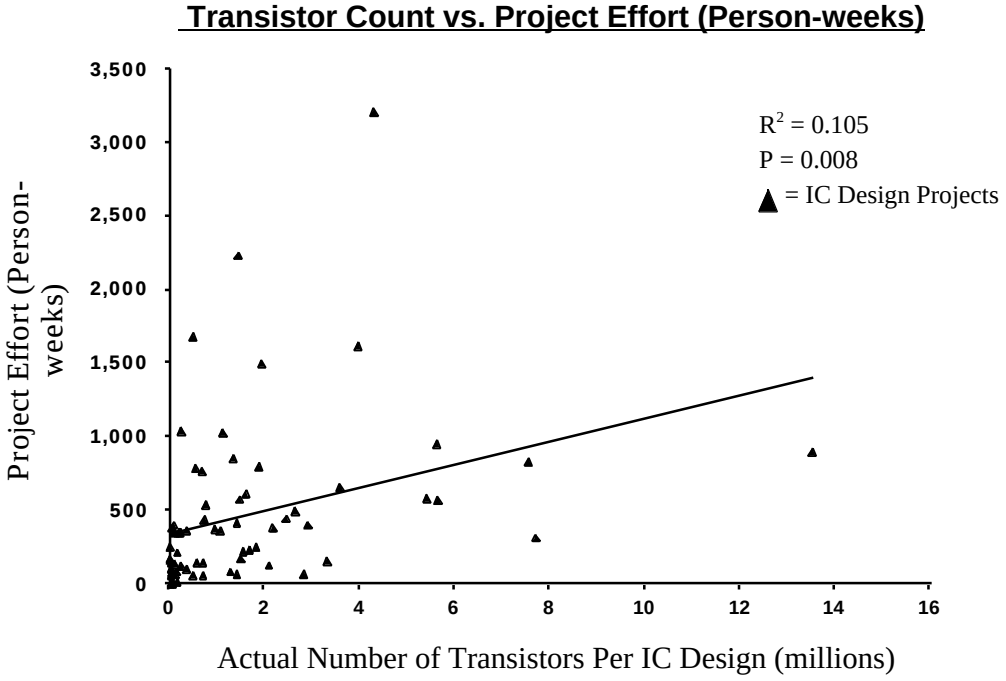

Figure 1. With an R^2 value of 0.105, the data illustrates that there is virtually zero correlation between engineering effort expended on chip design and the total number of transistors in the design. As shown, many large designs require significantly less effort than many small designs. Likewise, many small designs require significantly more effort than many large designs.

Numetrics Management Systems, Inc. has developed a set of proprietary techniques, referred to as the Normalization Methodology™ (patent pending), which achieves this goal. Normalization algorithms accurately quantify chip complexity across dissimilar projects, irrespective of device application, design methodologies, EDA tools, design flows, design practices or team composition. Normalization quantifies complexity by taking into account all major factors that influence complexity. It then calculates the number of "complexity units" for each chip.

III. Fair Comparisons: The Key to Measuring Productivity

Accurately measuring IC design productivity implies comparing the engineering performance of one project team against the performance of others. Thus, ensuring a fair comparison is a prerequisite to achieving accuracy—*i.e.*, comparing "apples to apples" so to speak. Fair comparison requires a two-prong approach. First, we must correctly quantify the relative complexity of all chips being compared, and this must be done consistently across all projects that we measure. As noted above, this requires a unit of measure that accurately quantifies complexity.

The second prong needed to accurately calibrate design productivity is to compare projects that are similar in characteristics. For example, we would like to group projects together that are similar in application, similar in design style, and similar in as many aspects as possible. The ability to do this depends on having a large database of projects.

The combination of the Normalization Methodology and grouping of similar designs overcomes the primary impediment to meaningful measurement of design team productivity and overall project team performance—namely, the inability to make fair and objective comparisons.

IV. The Numetrics Normalization Methodology

Normalization is critical to measuring productivity. Earlier we introduced the notion that engineering effort is a proxy for complexity. As such, the first step toward accurately measuring complexity is to examine those characteristics of a chip that impact engineering effort. These include things such as circuit type, timing constraints, amount of reuse, architecture, silicon density, firmware and so on. If we identify all of the major complexity attributes and develop accurate weighting factors for each, we have the beginnings of a methodology for quantifying complexity.

Once we have accurate weighting factors for all attributes, we apply them to the chip whose complexity we wish to measure. Next we can calculate the number of "complexity units" of the target chip, which is a quantitative representation of its complexity. This is the approach that Numetrics' Design Productivity Management System™ (DPMS) uses to perform normalization.

Critical to normalization are both identification of the primary complexity attributes and development of accurate weighting factors. CII has worked with companies and design teams throughout the electronics industry for many years to identify the critical attributes. The DPMS uses a proprietary approach, which is part of the Normalization Methodology™, to derive accurate weighting factors for all major complexity attributes.

The Normalization Methodology generates a complexity unit called a Normalized Transistor™ to quantify chip complexity—the greater a chip's complexity, the higher the number of Normalized Transistors™. A Normalized Transistor is a complexity unit. It is not a transistor.

Again, the DPMS uses its weighting factors to determine precisely how many Normalized Transistors to assign to a particular chip design. The number is based solely on the nature of the chip's complexity attributes.

Let's now apply the Normalization Methodology to the design projects in Figure 1 shown earlier, thereby calculating a Normalized Transistor count for each design, and re-plot the data. In this new graph, shown in **Figure 2**, the x-axis is the Normalized Transistor count, and the y-axis is again the effort expended to develop the chip. Here we get a dramatically different result from **Figure 1**.

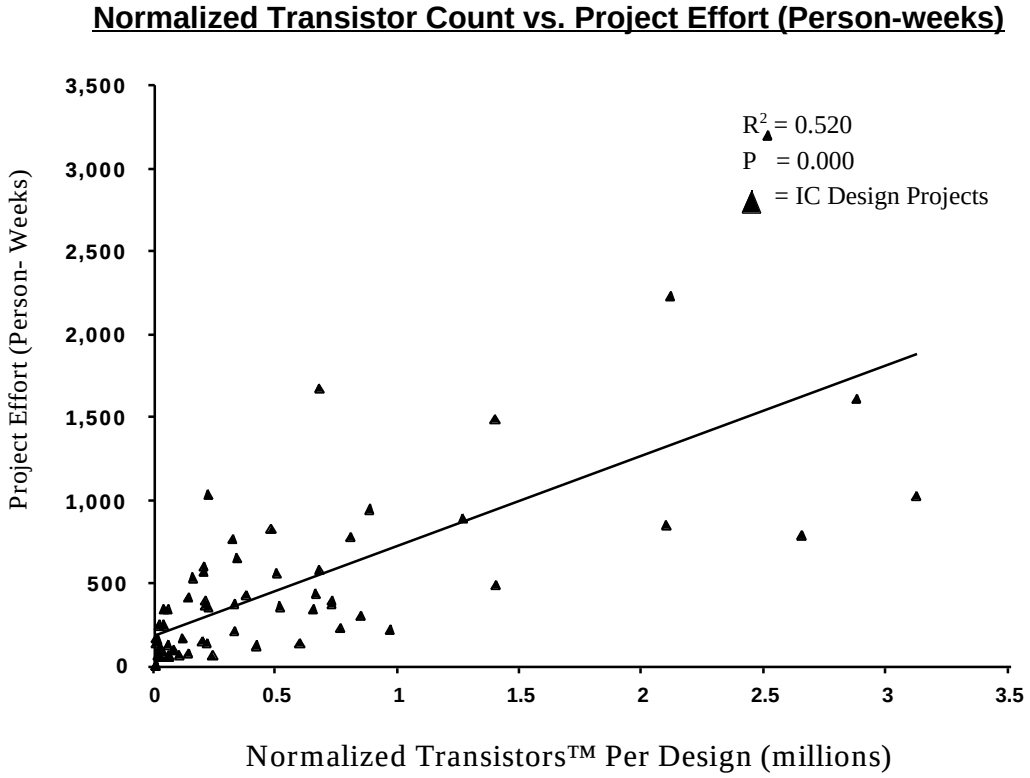

Figure 2. With an R^2 value of 0.52, the data illustrate that there is good correlation between engineering effort expended on chip design and the Normalized Transistor count calculated for a particular chip. Of the total engineering effort expended, 52% can be attributed to the inherent complexity of the chip design itself. Factors that influence the remaining 48% include engineering skills, design tools/flows/methodology, leadership and external factors that are often unpredictable.

Figure 2 shows that there is a high correlation between Normalized Transistor count and the amount of engineering effort expended to design a chip. Specifically, the R^2 factor, which is a reflection of how well the data fit the line, which is generated through a least squares regression analysis, is 0.520. Thus, 52% of the engineering effort expended can be attributed to the inherent complexity of a chip. This approach to measuring complexity gives DPMS users the means to quantify the true level of design complexity of their chip design projects.

Once we can accurately and quantitatively measure complexity, we have the foundation for an accurate measurement system. The following equation defines the Numetrics' productivity metric:

Design Productivity = Normalized Transistors / Person-Week

Other important metrics that engineering managers must monitor include time-to-market, development cost and reuse leverage. The DPMS calculates these and others and normalizes them whenever necessary to make fair and accurate comparisons.

V. Accuracy of Normalization

Figure 2 showed that 52% of the engineering effort expended can be attributed to the inherent complexity of a chip. Is this correct? The answer is yes, because this figure is generated though rigorous statistical analyses. Another way to think about the accuracy is to consider what factors contribute to the remaining 48%.

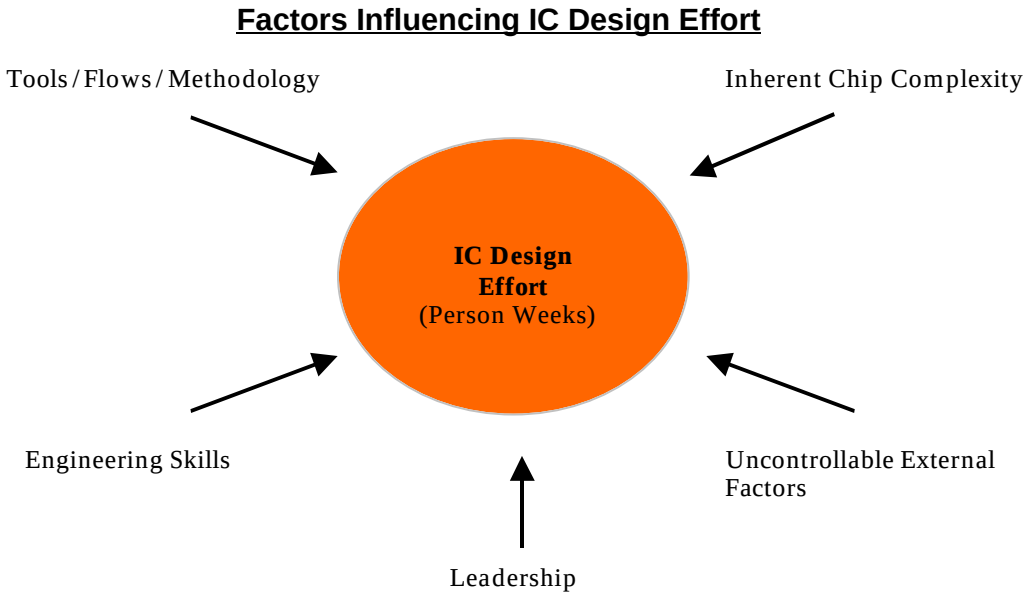

Figure 3. The amount of IC design effort expended on a project depends on inherent chip complexity, engineering skills, tools / flows / methodologies, leadership and uncontrollable external factors.

As **Figure 3** highlights, the amount of engineering effort, and therefore productivity, depends not only on chip complexity, but also on engineering skills, design tools, flows and methodology, management and "external factors" that are often unpredictable.

Since these factors typically have a substantial influence on the amount of effort expended on a project, we would not expect inherent chip complexity alone to account for much more than 52% of engineering effort. As a result, we can conclude that our intuition, combined with our statistical methods for quantifying chip complexity, leads to an accurate and effective measure of design productivity.